BEYOND-CMOS LOGIC AND INTERCONNECT USING COLLECTIVE PHENOMENA OF MAGNON, SKYRMION AND PLASMON

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Sourav Dutta

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BEYOND-CMOS LOGIC AND INTERCONNECT USING COLLECTIVE PHENOMENA OF MAGNON, SKYRMION AND PLASMON

Approved by:

Dr. Azad Naeemi, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Jeffrey A. Davis
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Arijit Raychowdhury
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Phillip First
School of Physics
Georgia Institute of Technology

Dr. Dmitri E. Nikonov
Components Research
Intel Corporation, Hillsboro

Date Approved: December 4th, 2017

To baba, ma and dida

(To my dad, mom and late grandmother)

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SUMMARY

The objective of this dissertation is to develop emerging beyond-CMOS logic and interconnect solutions using two alternative tokens for information processing - electron spin and plasma oscillation. Particularly, this research focuses on three collective phenomena, otherwise known as quasi-particles -magnons, skyrmions and plasmons. Following a bottom-up approach, this research diverts from the conventional route of building complementary logic gates (such as NAND, NOR) out of devices that behave like gated-switches. Instead, the work explores the possibility of deriving complex logic gates from functionally-enhanced devices by exploiting the wave-nature of magnons and plasmons for computing. Specifically, the innate majority-voting capability has been utilized for building majority logic gates that can enable efficient representation of circuits for complex computation functions. In the field of magnon-based data processing, the integration of magnetoelectric effect provides the possibility of low power excitation/detection, non-volatile memory, and wave-pipelining using clocking. The additional requirements for logic application like amplification, concatenability, non-reciprocity, complete set of Boolean operations and robustness with respect to thermal fluctuations (for spintronic-based devices) have been explored in this dissertation. The choice of a novel logic device demands a compatible fast and energy efficient interconnect technology. Information transmission via magnonic and plasmonic interconnect have been utilized to complement the respective logic gates at the local level. At the intermediate level, a more robust and effective solution is required to provide ultra-low power dissipation with high throughput. A skyrmion-based interconnect technology has been introduced in this dissertation, compatible with spintronic-based logic. Key topics like information transmission (write data), propagation, detection (read-out data) and signal transduction have been discussed with respect to both logic and interconnect.

CHAPTER 1
INTRODUCTION

1.1 Silicon Technology

The silicon-based semiconductor industry has been an ever growing corporation, starting from its inception around 1960s to a new worth of $335.2 billion in 2015. Such a revolutionary growth has been made possible due to the constant miniaturization of the feature size, resulting in improved performance, lower power dissipation and reduced cost per transistor. Today's Intel Core i5 processor, working at 14 nm technology node, shows a 3500$\times$ increase in performance, 90000$\times$ increase in energy efficiency and 60000$\times$ decrease in price per transistor compared to the first commercially available microprocessor 4004 [1]. The foundation for the constant scaling of CMOS (complementary metal oxide semiconductor) transistors was laid down by Gordon Moore in 1965 with an observation that *"the number of electronic components per integrated circuit would double every year for the following ten years"* [2]. Reassessing his earlier prediction and looking forward to the next decade, in 1975, he revised the forecast to *"the number of components per chip doubling every two years"* [3]. Initially proposed in the form of a mere engineering economics observation, Moore's Law later became a guiding principle and continued to shape the semiconductor industry for over 50 years. This phenomenal scaling not only enabled new innovative devices and applications with 25-30 $\%$ reduction in the cost of the transistor per year, but provided faster circuits with lower power dissipation. Within this time-frame, the number of transistors on a chip exploded from hundreds/cm^2 to approximately 7.2 billions on a single 22-core Intel Xeon Broadwell-E5 chip working at 14 nm in 2016 (see Figure 1.1).

The rapid penetration of information technology into new application domains beyond

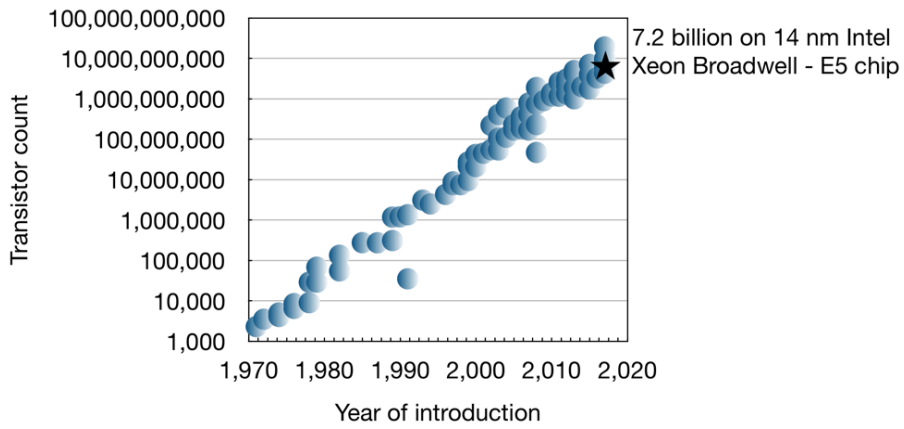

Figure 1.1: Enormous growth of the number of transistors on a chip.

just individual smart phones and laptops that enables the era of the Internet of Things (IoT) demands aggressive reduction of the size and the cost of the fundamental computing block - the CMOS transistor. However, as the size approaches tens of nanometer and below, transistor scaling faces several roadblocks arising from physical scaling limitation and limitation due leakage-induced escalating power density. The fundamental limitations on the minimum switching energy/bit and device size imposed by the laws of thermodynamics, quantum mechanics and communication theory indicates the end of the scaling roadmap for an electron-charge based binary switch. This raises the question of *"what new physical mechanism and technology may be explored and adapted to supplement and augment CMOS for continued scaling of information-processing technology"*.

1.2 Transistor Scaling

1.2.1 Physical and Power Limit

Marching at the same pace of Moore's law required constant technology innovations. As shown in Figure 1.2(a), the continued advances in technology has seen a transition from bipolar to MOSFETs, to CMOS, and significant innovations thereafter in CMOS including channel mobility enhancement using strained silicon [4–6]. Traditionally, the performance of CMOS transistor has improved with scaling at each technology node due to better

gate-control of transistor channel. However, as the channel length decreases, various short channel effects begin to diminish the performance of the transistor. The most prominent is the drain-induced barrier lowering (DIBL) which dramatically increases the subthreshold leakage currents. One way to mitigate DIBL is to improve the gate capacitance by reducing the oxide thickness which, however, gives rise to unwanted gate leakage current beyond a thickness of 2 nm due to direct quantum-mechanical tunneling from the gate to the channel. In an effort to achieve large gate capacitance, high-κ dielectrics like Hf and Zr have been introduced to replace SiO_2 [7–9] in high-κ/metal gate structure, followed by non-planar structures such as FinFET to further enhance the gate-to-channel control [10, 11]. Further improvement can potentially be achieved by introducing III-V compounds with high electron mobility property [12–14], germanium (Ge) FinFET [15], gate-all-around (GAA) or nanowire structure [16–19], carbon nanotube FET (CNT-FET) [20–22] and 2D materials, see Figure 1.2(b). However, a technology node beyond 10 nm would be significantly affected by direct quantum mechanical tunneling from the source to the drain [23].

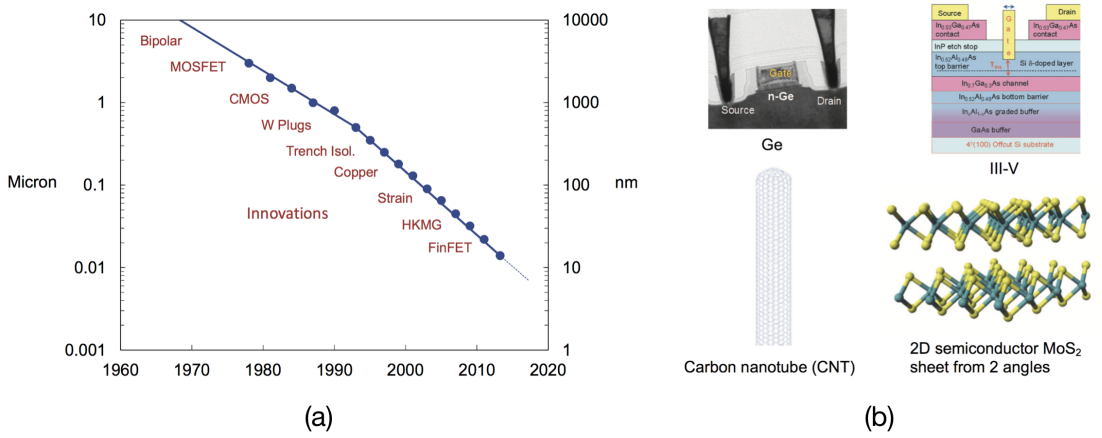

Figure 1.2: (a) Technology innovation driven by Moore's law. (b) Transistors with New Materials. Adapted from [1]

The crucial problem faced by today's silicon industry is the escalating power dissipation as shown in Figure 1.3(a). According to Dennard 's scaling, with each technology node, frequency f increases as $\propto 1/L_{gate}$, chip area decreases as $\propto 1/L_{gate}^2$ and the power density $\propto$ constant [24]. Following this law allowed the silicon industry to drastically increase the

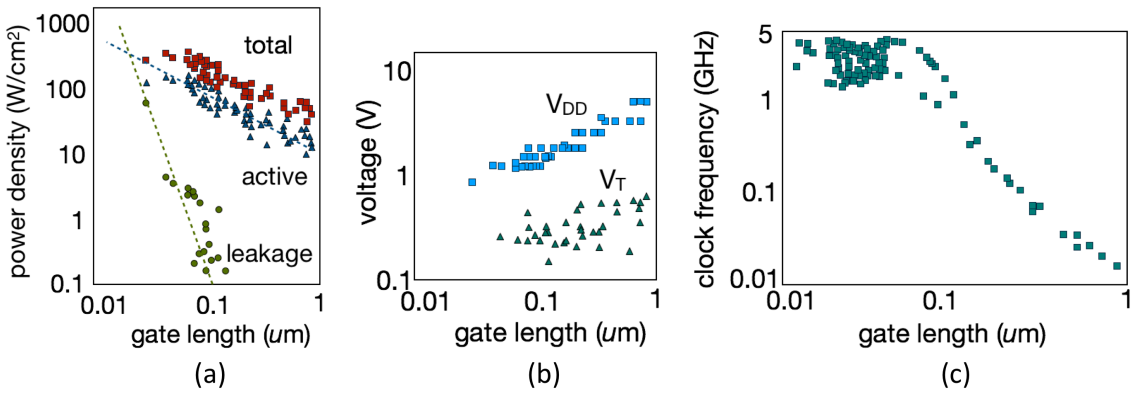

Figure 1.3: (a) Active-power density and subthreshold-leakage-power density calculated vs gate length. Adapted from [24]. (b) Scaling of supply voltage V_{dd} and threshold voltage V_{th} with gate length. Adapted from [24]. (c) Scaling of clock frequency with gate length. Adapted from [25].

clock frequencies from one generation to the next without significantly increasing overall circuit power consumption. However, around 2006 marked the end of this scaling roadmap causing a stagnation of the operating clock frequency ($\sim$ 3.5 GHz) and operating supply voltage ($\sim$ 1 V) [25] as shown in Figures 1.3(b) and (c), respectively. The primary reason is associated with the increase in the static power dissipation which, contrary to the scaling law, actually caused power density to increase by a decade. The power consumption can be classified into two categories: dynamics and static power. The dynamic power dissipation is associated with the charging and discharging of the processor's capacitive loads and scales with voltage V as $P_{dyn} \propto V^2$ and with frequency f as $P_{dyn} \propto f$. The static power on the other hand is associated with the power dissipation during the "off" state of the device and arises from two major sources of leakage current: sub-threshold leakage and gate leakage. Dennard's scaling demanded the operating voltage to scale with gate length and in order to maintain a high ratio ($> 10^6$) of current between the "on" and "off" states, the threshold voltage V_{th} will scale accordingly. However, the reduction of V_{th} leads to pronounced sub-threshold leakage currents, which significantly increases the static power dissipation (see Figures 1.3(a)). It is found that the leakage currents can be increased by 10 times if the reduction of V_{th} is about 85 mV [26].

1.2.2 Fundamental Limitation on Binary Switching

While the technology innovations have been driven steadily by scaling for the past 50 years, it is crucial to examine *"What are the limits to the maximum speed, maximum density and minimum energy of a system of binary switches?"*. The fundamental limit on the energy dissipation during a binary switching transition is given by the Shannon-von Neumann-Landauer (SNL) limit $E_{bit} = k_B T ln(2)$, where where k_B is Boltzmanns constant. The limit can be independently derived from there different perspectives: (1) thermodynamics put forward by John von Neumann, (2) quantum mechanics using a particle in a bistable potential well proposed by Landauer and (3) Shannons communication theory [27]. Based on the Heisenberg uncertainty principle, one can also estimate the the minimum size of 1.5 nm and switching time of 0.04 ps for a binary switch. Zhirnov et al. [28] pointed out that the SNL value for minimum switching energy underestimates the minimum switching energy required to operate the device. Incorporating the tunneling probability of electron within the Wentzel-Kramers-Brillouin (WKB) approximation in the two-well, one-barrier model, the generalized value for minimum energy per switching operation at the limits of distinguishability that takes into account both classic and quantum transport phenomena is given by $E_{bit} \approx k_B T ln(2) + \frac{\hbar^2 (ln2)^2}{8ma^2}$, where a is the barrier width and m is the effective mass. It is seen that for $a > 5$ nm, the modified expression agrees with the SNL limit, while for $a < 5$ nm, the minimum switching energy becomes considerably larger. A later work by Nikonov et. al. [29] following the approach of Zhirnov et al. with few modifications determined the fundamental limits of electronic computing as: E_{bit} = 77.6 meV and a = 3.8 nm. With the current CMOS technology moving towards these fundamental limits, any further reduction in the energy consumption has to incorporate new state variables apart form the electron charge. With 14 nm technology node currently being used, it is anticipated that the 5 nm generation may follow in 2020. Consequently, scaling of CMOS technology will face fundamental limits within the next few years. This determines a need to have new technology options for extending CMOS and the search for alternative information processing

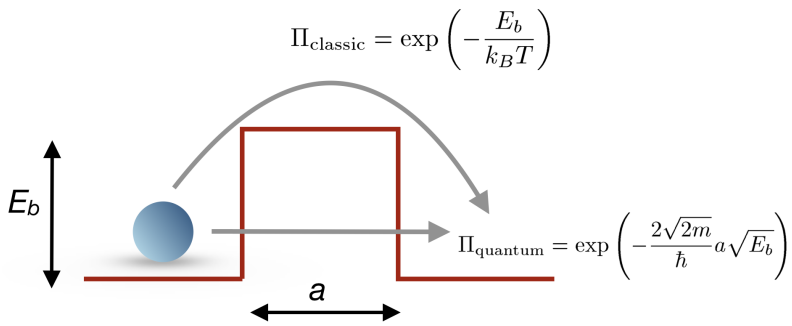

Figure 1.4: Two-well model for illustrating limitation on binanry switching. The two states represent bit "1" and "0". There are two probabilities for spontaneous transition from one state to another: classical and quantum mechanical.

paradigm that considers new "tokens" to replace the electronic charge.

1.3 Interconnect Technology Scaling

Smaller and faster transistors must be complemented by a fast and energy efficient interconnect technology to develop high performance microchip. The quintessential purpose of an interconnect is to communicate information between different physical locations on the chip with minimum latency [30]. However, as the number of transistors on a chip increased, so did the number of interconnections that are required to maintain communication. Contrary to the early interconnect problem, today's silicon industry faces a different challenge associated with (a) routing the tremendous number of wires on a microchip in the same footprint and (b) latency and performance issue associated with the interconnects at newer technology nodes. The intrinsic latency of an RC interconnect is proportional to $\tau \propto L^2 r_w c_w \propto \rho\epsilon L^2/HT$, where L is the interconnect length, r_w and c_w are the resistance and capacitance per unit length, ρ is the metal resistivity, ϵ is the permittivity of the dielectric, and H and T are the metal heingth and insulator thickness, respectively. Possible options to reduce the interconnect delay involves reducing ρ using new materials, scaling ϵ, reducing L using novel architectures, and reverse scaling H and T. Since 220 nm technology node, copper has been the backbone for interconnect technology. In current

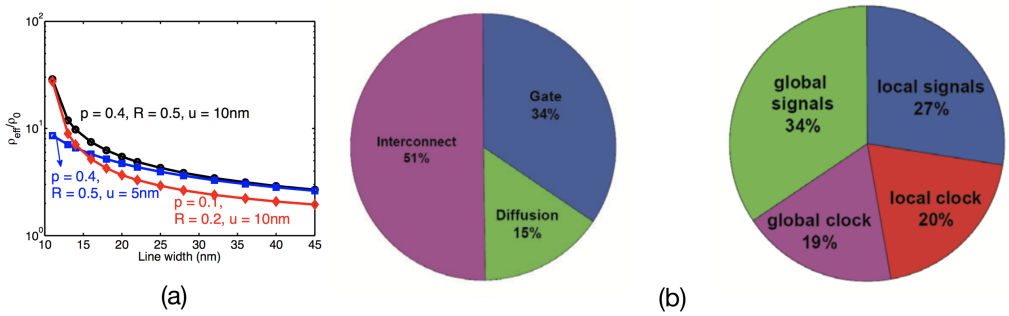

Figure 1.5: (a) Resistivity of Cu line normalized to the bulk resistivity of Cu versus linewidth Adapted from [34]. (b) Total dynamic power breakdown and power breakdown by types. Adapted from [35]

CMOS technology, switching to the Cu/lowκ interconnect technology introduced a lower $\rho\epsilon$ product improving the performance of the interconnect. Furthermore, in effort to reduce the capacitance, progressively lower-κ dielectric materials have been introduced in many generations of technology [31]. The 22-nm technology node comprises 9 Cu layers with an ultralowκ dielectric material [32]. However, post-22 nm technology node posses a radical change in the behavior of the local interconnects. At such scaled dimensions, the resistivity of Cu interconnects significantly increases due to size effects, such as sidewall and grain boundary scatterings, and line edge roughness (LER) [33] as shown in Figure 1.5(a). This radical change in Cu interconnect limitations for ultra-scaled future technology nodes motivates looking at alternative interconnect technologies that can replace Cu at the local metal levels.

Another motivation for focusing on interconnect comes from the significant portion of the power dissipated in a microprocessor being associated with the dynamic power dissipated in interconnects. An interconnect power analysis study performed on a microprocessor designed for power efficiency, consisting of 77 million transistors, and fabricated in the 0.13 μm technology in 2004, revealed that interconnects account for 50$\%$ of the total dynamic power dissipation [35, 36] (see Figure 1.5(b)).

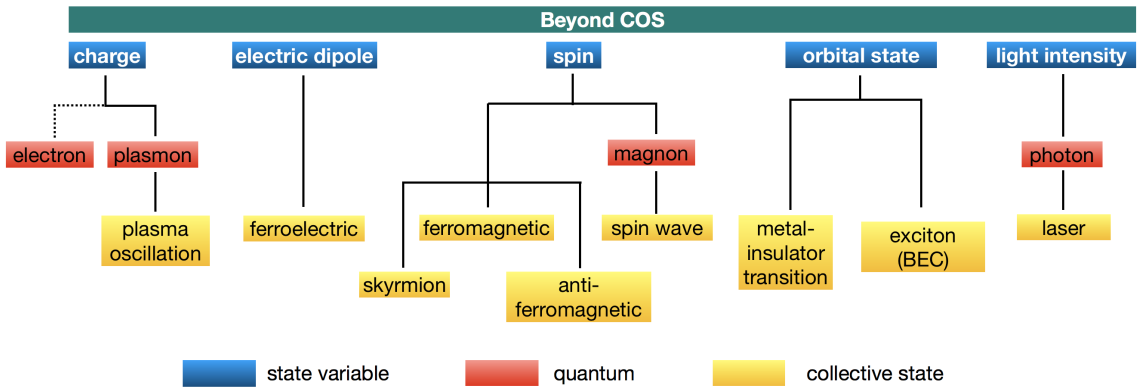

Figure 1.6: Illutration of beyond-CMOS state variables and devices [37].

1.4 Beyond-CMOS

With the dimensional scaling of CMOS approaching the fundamental limits, several new alternative "tokens" for information processing, novel devices and micro-architectures are being explored that can potentially extend/augment the existing CMOS technology as well as add new functionality to sustain the historical scaling of integrated circuit and reduction of cost/function in future decades. These new information processing devices and architectures are often called Beyond-CMOS technologies.

1.4.1 Alternative Computational Variables

The beyond-CMOS devices encode information using various physical quantities which we call the "computational variables" or "state variables". Figure 1.6 highlights the various state variables like charge, electric dipole, spin, orbital state and light intensity. In traditional charge-based devices (shown by the dotted line in the Figure), the presence or absence of electrons is used to denote logic "1" and "0", respectively. Non-traditional beyond-CMOS devices aim at utilizing various other physical quantities and often collective states like ferromagnetism, ferroelectricity etc. which provide added advantages like non-volatility or energy-efficient operation. A comprehensive overview of beyond-CMOS devices can be found in [38–41] and the references therein. Of particular interest in this

thesis are collective excitations (often referred to as "quasi-particles") which are emergent phenomena and low-lying excited states of a system. Based on electron spin, our topics of discussion will be *"spin wave"*, or its quantum - *"magnon"*, which is a collective precession of spins and *"skyrmion"* which is a topologically non-trivial spin texture. Based on electron charge, we will discuss *"plasma oscillation"*, or its quantum - *"plasmon"*, which is a collective oscillation of electron density at the interface of a metal and a dielectric.

1.4.2 Emerging Logic

Non-conventional charge-based devices incorporate novel mechanisms to manipulate and transport electron charge. Among this group, worthy of mentioning are tunnel FETs (TFETs) that rely on band-to-band tunneling (BTBT) for conducting current [42] and negative-capacitance FET (NC-FET) that uses ferroelectric instead of standard gate insulator [43]. The goal is to achieve steeper sub-threshold slopes < 60 mV/decade.

The possibility of using electron spin as a computational or state variable for logic devices and circuits has been the focus of research lately [44]. Active research in the field of spintronics gained momentum following the discovery of the giant magnetoresistance (GMR) independently by Albert Fert et al. [45] and Peter Grunberg et al. [46] for which they were awarded the 2007 Nobel prize in physics. Spintronics came into mainstream electronics due to the pioneering work of integrating GMR read-heads in hard-disk drives by IBM in 1997 which allowed tremendous increase in data storage density over the past years. In *"ferromagnetic spintronics"* [1], typically a bi-stable nano-magnet is used where logic "1" and "0" are assigned to the two ground states of the magnet, separated by an energy barrier. The energy barrier is often an inherent property associated with the nano-magnet which can be exploited to retain the magnetization state, thus enabling non-volatility. A quintessential spintronic logic can be envisioned to be composed of three generic components: (a) a write

[1] Ferromagnetism is chosen as one of the subject matters of this thesis. However, the area of "antiferromagnetic spintronics" is also an equally growing research field now and lies beyond of the scope of this thesis.

unit (input), (b) a read unit (output) and (c) a channel for communicating information between the write and read unit. The data can be written using various physical phenomena starting from traditional spin-transfer torque (STT) [47] to more energy efficient choices like spin-orbit torque (SOT) [48, 49] and magnetoelectric (ME) effect [50]. Information read-out is generally achieved using the GMR or tunnel magnetoresistance (TMR) [51] effect in a magnetic tunnel junction (MTJ), although alternative strategies like the inverse-ME (iME) effect and inverse-spin Hall effect (iSHE) [52, 53] are being investigated to improve performance and robustness. Among the various candidates within the spintronic logic family, spin wave logic will be the focus of subsequent discussion in this thesis. A more comprehensive review of other potential candidates like nanomagneic logic (NML), all spin logic (ASL), strain-based devices, spin torque devices and domain wall logic can be found in the review articles [38–41] and the references therein.

Ferroelectrics, utilizing the electric dipole as the state variable, provide an attractive option for non-volatile beyond-CMOS devices including ferroelectric transistor (FeFET) and memory (FeRAM)). This material class also has a significant overlap with the field of spintronics, giving rise to magneto-electric effect which will be a topic of discussion in this thesis. Another candidate is utilizing excitons which are electrically neutral quasi-particles composed of bound states of electrons and holes tied together by the Coulomb force.

Although not included within the Nanoelectronics Research Initiative (NRI) benchmarking effort of Semiconductor Research Corporation (SRC) on beyond-CMOS devices [38, 40], plasmons are an attractive state variable. Plasmons are quanta of oscillating electron density. They can remain confined at an interface between a metal and a dielectric forming *"surface plasmons"* and interact strongly with light resulting in a *"surface plasmon polariton (SPP)"*. SPP waves exhibit a much shorter wavelength compared to light at the same excitation frequency and hence can confine light in feature size beyond the diffraction limit [54, 55]. This can help in the miniaturization of photonic circuits to provide to high-bandwidth dense on-chip integrated logic circuit.

1.4.3 Emerging Interconnect

Any novel logic device technology must be complemented by a fast and energy efficient interconnect technology. Interconnects have proved to be a limiting factor for the power efficiency and performance for silicon CMOS chips. This highlights the fact that interconnects cannot be treated as an afterthought while investigations are being made for new information processing elements. Moreover, a signal transduction between charge and spin (or other state variable) is costly both in terms of energy and area, and must be avoided if possible. At the local level, the boundary between logic device and interconnect is blurring. In other words, most of these devices perform both the task of computation as well as communication [56–58]. Hence, at the local level, a logic technology can be complemented by the respective interconnect technology. However, at the intermediate level where communication is the main aim, a more robust and effective solution is required to provide ultra-low power dissipation with high throughput.

Communication between devices on the chip can be categorized into two major transport modes: particle-based transport and wave/collective phenomena-based transport. Transport mechanisms involving diffusion, drift, and ballistic transport using electron charge, spin, exciton and phonon fall into the category of particle-based communication. Wave/collective phenomena-based communication involve plasmonic waves, spin waves (or magnons), domain walls and skyrmions. In this thesis, we focus on collective phenomena of magnons, plasmons and skyrmions for signal transmission and communication.

1.5 Emerging Computing Architecture

1.5.1 Beyond-CMOS as Drop-In Replacement

Figure 1.7(left) shows the conventional paradigm for chip design following a bottom-up approach. Starting with the state variable (traditionally electron charge) and the choice of appropriate materials, the main focus of the device community has been the quest for an

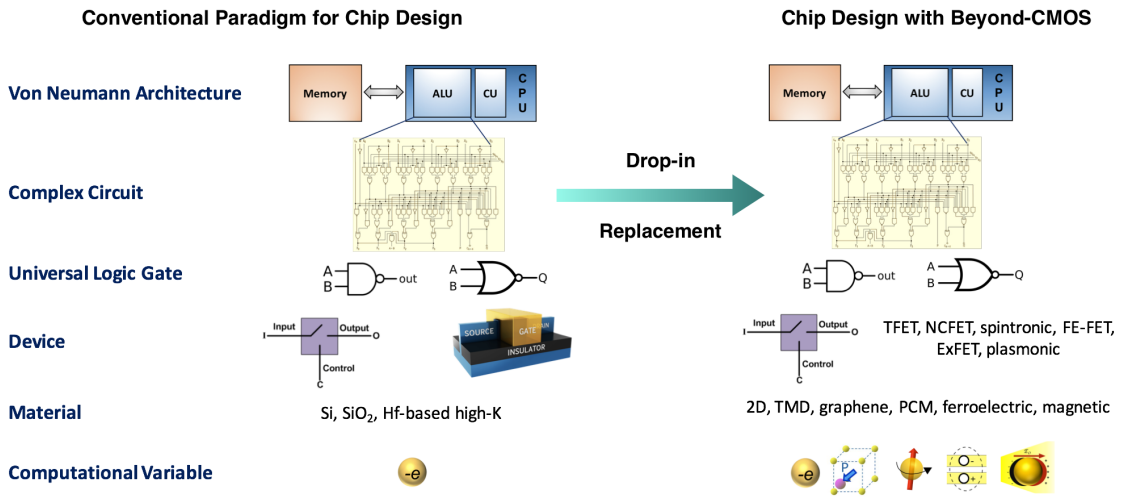

Figure 1.7: Illustration of conventional paradigm for chip design and notion of using beyond-CMOS devices as a drop of replacement at the lower levels.

ultimate switch which is often envisioned as simply a single gated device. The rest of the chip design then incorporates building universal NAND-NOR logic gates, cascaded them into multiple levels to build complex logic circuit that form blocks like ALU. Traditionally, the Von-Neumann architecture is used at the top level where the memory and the CPU are separated. The notion of using beyond-CMOS devices has often been a drop-in replacement of CMOS at the bottom level as shown in Figure 1.7(right), while the rest of the paradigm for chip design remains the same. However, its has been seen using extensive benchmarking efforts that as one goes up this stack, some of the advantages provided by these novel devices is lost. In other words, as Shabadi and colleagues [59] have put it, system-level performance may not proportionally scale with the individual device performance. The question then arises *"can these devices offer more computing abilities than simple switches to improve system-level performance or better application specific computing operations?"*.

1.5.2 Rethinking the Bottom-Up Approach

The fundamental question stated above allows one to rethink the conventional bottom-up approach. As shown in Figure 1.8, diverting from the conventional route of building complementary logic gates (such as NAND, NOR) out of devices that behave like gated-switches, one can envision building functionally-enhanced devices out of the alternative state variables and exotic materials. These functionally enhanced devices will be capable of performing arbitrary logic functions with high fan-in and fan-out, and give rise to complex logic gates which are *"nano-function"*. A simplest example would be majority logic gate with 3 inputs. In this way, we can move the level of abstraction from a gated-switch to a nano-function, and build complex circuits out of them. At the highest level, a traditional Von-Neumann architecture may be followed, or one can explore other emerging computing architectures like co-located memory-logic, cognitive computing, stochastic computing and using collective-effects like coupled oscillators. In this way, we can expand the entire nano-device and system design space.

Wave-Based Computing

Several members of the beyond-CMOS family like magnons and plasmons exhibit wave nature that can be exploited for computing. Especially, the innate majority-voting capability can be utilized for building majority logic gates that can be treated as nano-functions for building more complex circuits. The principle phenomena guiding wave-based computing is interference of waves. Consider a propagating wave $S = S_0 e^{i(kx-\omega t+\phi)}$ where S_0 depends on the stimulus at the point of excitation, ω is the frequency and k is the wave-vector. The phase of the wave ϕ can be considered as the state or computational variable. The information bit can then be encoded in the phase of the wave such that a phase "$\phi = 0$" represents a logic "1" and a phase "$\phi = \pi$" represents a logic "0". In general, consider an odd number of input waves interfering in a combiner region. If m is the number of inputs with phase "$\phi = 0$" and n is the number of inputs with phase "$\phi = \pi$", the resultant wave

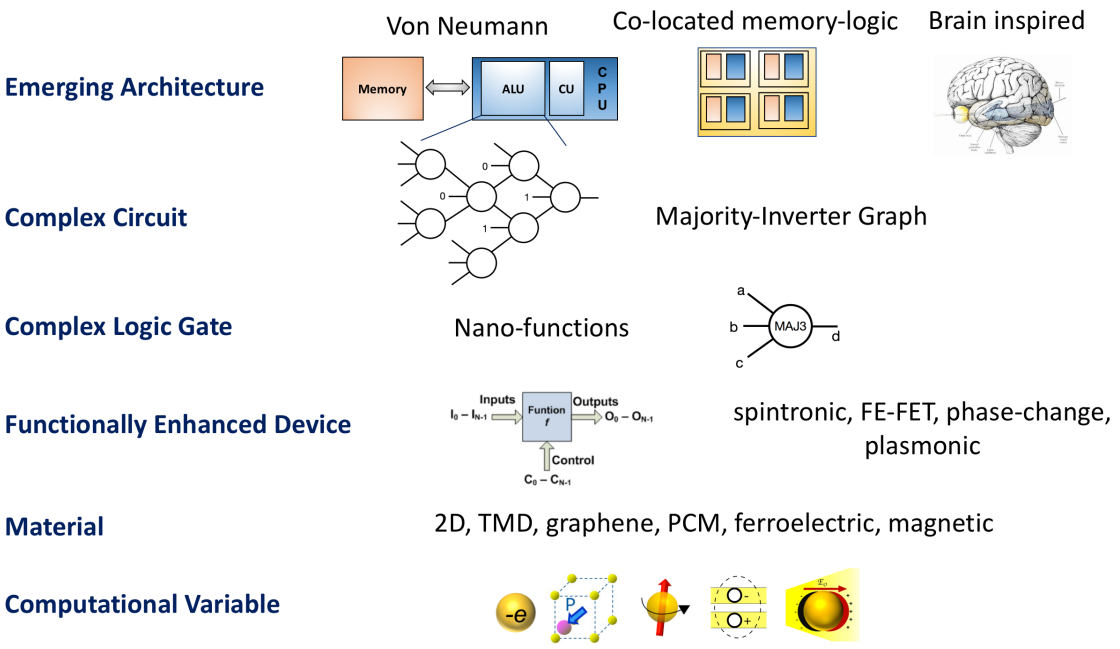

Figure 1.8: Rethinking the bottom-up approach that can enable the devices to offer more computing abilities than simple switches to improve system-level performance or better application specific computing operations

can be approximated as $S_{out} = (m-n)S_0 e^{i(kx-\omega t+\phi)}$. Such a wave-based computing using an odd number of inputs displays an inherent *"majority voting"* capability and helps in the efficient realization of a *"majority logic gate"*. Figure 1.9 shows the schematic of a 3-input majority logic. The output phase becomes a majority of the phase of the input waves. Additionally, the peak amplitude depends on the number of inputs with phases "$\phi = 0$" and "$\phi = \pi$" as $S_{out} = (m-n)S_0$, hence denoting the strength of the majority. In a 3-input majority logic, the strongest majority displays an output amplitude $3\times$ larger than the input waves (see Figure 1.9). A critical requirement of such wave-computing utilizing the phase as the state variable is to have odd number of inputs. An even number of inputs would possibly result in a complete destructive interference (with no output signal) giving rise to an in-determinant state. Alternative to wave-based computing focused on performing digital operations, wave-based neuromorphic computing with nano-device have also been proposed [60]. Owing to lower energy dissipation, magnonss can prove to be a promising candidate in this field.

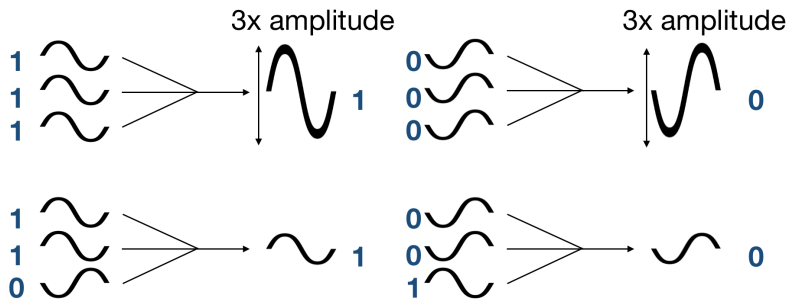

Figure 1.9: Illustration of wave-based computing using an example of 3-input majority logic.

Majority-Interver Graph

Deviating from the traditional path of CMOS oriented chip design, new logic abstractions and synthesis techniques are being developed for the emerging nano-devices that are capable of reproducing the same CMOS logic circuitry with lower footprint and higher performance with only two building blocks - inverter and majority logic gate [61, 62]. Such novel logic abstractions and synthesis techniques fully utilize the innate expressive power of the nano-devices and as such may unlock the true potential of various beyond-CMOS candidates, otherwise hidden by plain synthesis methodologies. Candidates like magnons and plasmons utilizing wave superposition and interference inherently poses an enhanced native functionality - the majority voter, and as such are again perfectly suited for such novel logic abstraction. Recent works have demonstrated that magnonic logic expressed using the majority-inverter graph (MIG) can provide advantages over traditional CMOS [63–66], even though the individual device may be inherently slower than CMOS. Similar investigation in the plasmonics domain are currently being performed.

1.6 Thesis Overview and Organization

The focus of this thesis is to develop emerging beyond-CMOS logic and interconnect solutions using two alternative tokens for information processing - electron spin and plasma oscillation. Particularly, this research focuses on three collective phenomena, otherwise

known as quasiparticles - magnons, skyrmions and plasmons. The work involves a bottom-up approach, undertaking investigations and motivating future work at various hierarchical levels - from computational variables to materials, devices, circuits and architecture. The vision in this work has always been not to replace CMOS but to augment them in order to add new functionalities and sustain the historical scaling of integrated circuits. The thesis primarily consists of three parts - magnonic logic, plasmonic logic and skyrmion interconnect.

The first part of the thesis focuses on magnonic logic. Chapter 2 discusses a comprehensive scheme of developing a clocked non-volatile magnonic logic device. The integration of the magnetoelectric (ME) cells with the spin wave bus (SWB) provides a possible route for low power excitation and detection of spin waves and for non-volatile memory element. A novel clocking scheme has been introduced to ensure uni-direction flow of signal and wave-pipelining. The re-generation of spin waves at each stage provide an automatic amplification to take care of the propagation loss. The question of robustness to thermal fluctuations along with possible strategies have also been discussed. Chapter 3 focuses on challenges that need to be addressed as we move up the stack from device to circuit level and build an entire spin wave logic circuit. It includes analysis of crosstalk noise, developing primitive logic gates like inverter and majority gate, energy-efficient transducer design for signal conversion and performance evaluation and comparison with CMOS.

The second part of the thesis comprising Chapter 4 extends the idea of wave-based computing to the field of plasmonic logic. Contrary to the state-of-the-art plasmonic logic devices that utilize the intensity as the state variable, here the phase of the wave has been used to develop nanoscale cascadable plasmonic logic gates. Key topics like trade-off between propagation loss and confinement, crosstalk noise and cascadability have been discussed along the development of nanoscale inverter and majority logic gates. The non-Boolean computational capability of the device has also been explored.

The third part of the thesis focuses on interconnect technology. Information transmis-

sion via magnonic and plasmonic interconnect have been utilized to complement the respective logic gates at the local level. However, at the intermediate level, a more robust and effective solution is required to provide ultra-low power dissipation with high throughput. Prior work on plasmonic interconnect have established that it may be possible to transmit information up to $\sim$ 100 μm via plasmonic interconnect before it becomes energetically unfavorable, and one needs to insert repeaters or switch to electrical interconnect [67]. Hence, in this thesis we do not focus further on plasmonic interconnect at the intermediate level. In the spintronic domain, a skyrmion-based interconnect technology has been introduced in Chapter 5, which proves to energy efficient compared to other contemporary spintronic interconnects in the intermediate regime. The chapter discusses three essential components of skyrmion interconnect - skyrmion nucleation, transport and read-out in a confined nanowire gerometry of sub-100 nm width and in material systems exhibiting low chirality.

CHAPTER 2
MAGNONIC LOGIC DEVICE

2.1 Background

2.1.1 Ferromagnetism

Magnetism is closely related to the angular momentum of an electron. The orbital motion of an electron around the nucleus generates an angular momentum called the *"orbital angular momentum"* and a resultant *"orbital magnetic moment"*. In addition, electrons have an additional intrinsic angular momentum independent of the orbital motion called *"spin angular momentum ($S = \hbar/2$)"*. The associated magnetic moment is termed *"spin magnetic moment ($\mu_S = e\hbar/2m_e$)"*. Spin is a quantum mechanical property of the electron arising from the Dirac equation and hence is difficult to provide an accurate picture of it. However, one can imagine the electron as a spinning top generating the "spin magnetic moment". According to quantum mechanics, the angular momentum vector of a $S = \hbar/2$ particle can be either parallel or anti-parallel with an arbitrarily chosen quantization axis. Usually z-direction is chosen as the quantization axis and the electrons are denoted as *"up-spin"* or *"down-spin"* depending on whether they are aligned or anti-aligned with it. In transition metals, electrons display spontaneous spin-polarization (spins aligned with a given direction) due to the competition between atomic-like exchange interaction, which tend to align spins, and inter-atomic hybridization, which tends to reduce spin polarization. The atomic-like exchange interaction can be qualitatively understood from Hunds rule and Pauli exclusion principle. On the other hand, in solids, electron states on neighboring atoms hybridize and form bands that act to suppress the formation of magnetic moments. The transition metal ferromagnets are of particular interest here owing to their partially filled d-orbitals. They display both strong exchange splitting and hybridization. The exchange splitting

stabilizes a spin-polarized (ferromagnetic) state in the presence of band formation by generating a shift of the majority-spin band to a lower energy than the minority-spin band (see Figure 2.1). The phenomenological description of magnetism, varying on a mesoscopic length scale, called "micromagnetics" has been described in details in Section 2.1.3.

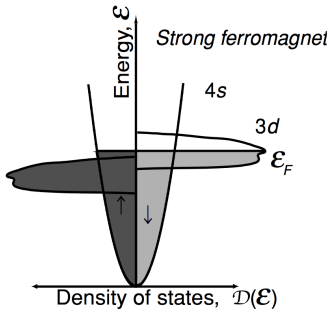

Figure 2.1: Densities of states for a strong ferromagnet. Adapted from [68].

2.1.2 Early History of Spin Wave

Spin waves are propagating disturbances in magnetically ordered materials, analogous to lattice waves in solid systems and are often described from a quasiparticle point of view as magnons. Although *"spin-based electronics"*, aka. Spintronics emerged around 1980s as an alternative idea to conventional electronics, the history of spin waves dates back to the early investigation of magnetism, purely from a physicist's point of view. Following Weiss's *"molecular field"* theory of magnetic ordering[1] in 1907, Heisenberg and Dirac laid the foundation of the *"exchange interaction J"* among neighboring spins responsible for the magnetic ordering in 1926. The zero-temperature ground state of a Heisenberg ferromagnet $|0\rangle$ is an eigen-state of the Hamiltonian

$$\mathcal{H} = -\frac{1}{2}J\sum_{i,j}\mathbf{S}_i \cdot \mathbf{S}_j - g\mu_B \sum_i \mathbf{H} \cdot \mathbf{S}_i \tag{2.1}$$

[1] In the absence of magnetic interaction, the individual magnetic moments in a solid will be thermally disordered at any temperature giving rise to zero net magnetization. Some solids, however, display non-vanishing average magnetic moment below a critical temperature T_C, called *"Curie temperature"*. Such solids are called *"magnetically ordered"*. In *ferromagnetic* materials, the individual magnetic moments add up to exhibit a macroscopic bulk magnetization density known as *"spontaneous magnetization M_S"*.

and is expected to be the one with all spins aligned parallel with each other and to the field H as shown in Figure 2.2(a). Variable g is the Lande-g factor, μ_B is the Bohr magneton and S is the spin at Bravais lattice. The individual mean spin S and saturation magnetization M_S are related as

$$M = g\mu_B \frac{N}{V} S \tag{2.2}$$

where N is the total number of Bravais lattice sites and V is the volume.

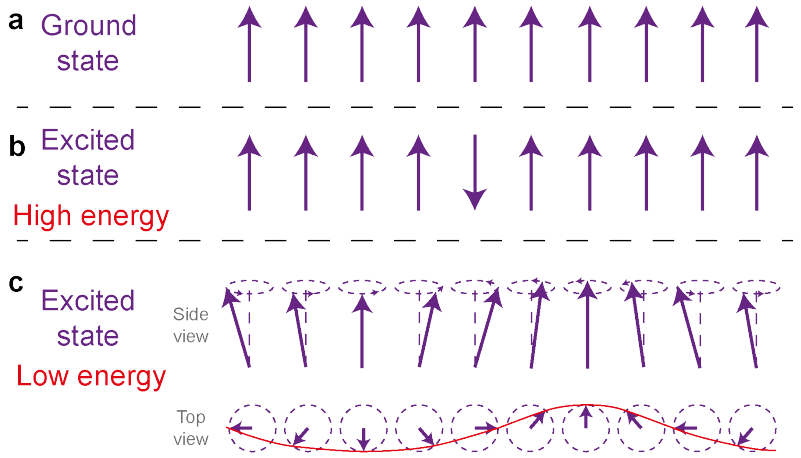

Figure 2.2: (a) Zero-temperature ground state of a Heisenberg ferromagnet where all spin are aligned. (b) Excited state of the ferromagnet with one spin flipped. (c) Excited state with a lower energy tcompared to (b) where the lowered spin is distributed among all the neighboring spins. The spins are precessing around their equilibrium, forming a spin wave or magnon

The concept of spin waves was introduced in terms of low-temperature behavior of Heisenberg ferromagnet. The low-lying or first excited state can not be simply represented as a state $|R\rangle$ differing for the ground state $|0\rangle$ such that only one spin at site R has its z-component reduced from S to $S-1$ (see Figure 2.2(b)). In fact, such a low energy state $|k\rangle$ is given by the superposition of states, each of which has the total spin NS reduced by 1.

$$|k\rangle = \frac{1}{\sqrt{N}} \sum_R e^{ik\cdot R} |R\rangle \tag{2.3}$$

This state is called a spin wave or magnon with wavevector k. The lowered spin is dis-

tributed among all the neighboring spins with probability $|\langle k|R\rangle|^2 = 1/N$. The microscopic picture of the state $|k\rangle$ is shown in Figure 2.2(c). This low-lying excited state of the ferromagnet laid the foundation of the Bloch $T^{2/3}$ Law which states that the spontaneous magnetization at temperature $T > 0$ will deviate from the saturation value by an amount proportional to $T^{2/3}$. The success of the proposed spin wave excitation was that the predicted Curie temperatures T_C was much lower than that expected from molecular field theory and matched very well with experiments.

2.1.3 Mathematical Description and Micromagnetic Modeling

Spin waves can be treated both as classical excitation as well as from quantum mechanical point of view. In this thesis, the focus has been on the classical approach known as *"micromagnetics"*. Micromagnetics is a phenomenological description of magnetism on a mesoscopic length scale. Rather than describing the behavior of magnetic moment associated with each atom, it adopts a continuum description similar to that of elasticity theory. A propagating spin wave can be described using the phenomenological Landau-Lifshitz-Gilbert (LLG) equation that describes the dynamics of the magnetization

$$\frac{d\vec{m}}{dt} = -\frac{\gamma}{(1+\alpha^2)}(\vec{m} \times \vec{H}_{eff}) - \frac{\alpha\gamma}{(1+\alpha^2)}[\vec{m} \times (\vec{m} \times \vec{H}_{eff})] \tag{2.4}$$

where $\vec{m}$ is the unit magnetization vector defined as $\vec{m} = \vec{M}(\vec{r})/M_s$, γ is the gyromagnetic ratio and α is the Gilbert damping parameter. In the absence of spin-torque[2], there are two torques that act on the magnetization: the precessional torque (first term) makes the magnet precess around an effective magnetic field $\vec{H}_{eff}$, and a damping torque (second term) that tends to align the magnetization with the direction of $\vec{H}_{eff}$ (see Figure 2.3). According to the theory of magnetics, the effective field $\vec{H}_{eff}$ can be calculated as a derivative of the

[2] see Section 3.4.1 for description of additional spin-torque terms

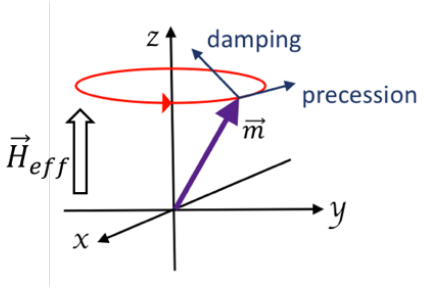

Figure 2.3: Magnetization dynamics governed by the Landau-Lifshitz-Gilbert (LLG) equation.

total energy E with respect to the magnetization as

$$\vec{H}_{eff} = -\frac{1}{\mu_0 M_s}\frac{\partial E}{\partial \vec{m}} \tag{2.5}$$

The total micromagnetic energy E consists typically of four main contributions: the exchange interaction among neighboring spins, anisotropy interaction due to spin-orbit interaction, Zeeman interaction due to applied external magnetic field H_{app} and magnetostatic or demagnetizing energy

$$E = \int_v \left[A(\vec{\bigtriangledown}\vec{m})^2 - K(\vec{m}.\hat{u})^2 - \mu_0 M_s(\vec{H}_{app}\cdot\vec{m}) - \frac{1}{2}\mu_0 M_s(\vec{H}_{demag}\cdot\vec{m}) \right] d^3r \tag{2.6}$$

where A is the exchange constant, K is uniaxial anisotropy, $\hat{u}$ is the unit uniaxial anisotropy axis, $\vec{H}_{demag}$ is the demagnetizing field. As defined above, the effective field can then be written as:

$$\vec{H}_{eff} = \frac{2A}{\mu_0 M_s}\bigtriangledown^2\vec{m} + \frac{2K}{\mu_0 M_s}(\vec{m}\cdot\hat{u})\hat{u} + \vec{H}_{app} + \vec{H}_{demag} \tag{2.7}$$

The demagnetizing field is expressed as

$$\vec{H}_{demag}(\vec{r}) = -\frac{1}{4\pi}\int_v \vec{\bigtriangledown}\cdot\vec{M}(\vec{r}')\frac{r-r'}{|r-r'|^3}d^3r + \frac{1}{4\pi}\int_S \hat{n}(\vec{r}')\cdot\vec{M}(\vec{r}')\frac{r-r'}{|r-r'|^3}d^2r \tag{2.8}$$

and can be simplified into a discrete form following the approach of [69] as $\vec{H}_{demag,i} = -\sum_j N_{i-j}M_s\vec{m}_j$, where N_{i-j} denotes the demagnetization tensor, depicting the demagne-

tization in cell i due to magnetization in cell j. The tensor is given by a 3×3 matrix and depends only on the distance between the ith and the jth cell.

$$N = \begin{bmatrix} N_{xx} & N_{xy} & N_{xz} \\ N_{xy} & N_{yy} & N_{yz} \\ N_{xz} & N_{yz} & N_{zz} \end{bmatrix} \tag{2.9}$$

The values of the tensor elements (e.g., N_{xx}, N_{xy}) can be evaluated using [69] and [70].

The concept of numerical micromagnetics is utilized to simulate spin wave dynamics in the publicly available code Object Oriented Micromagnetic Framework (OOMMF) [71]. In numerical micromagnetics, the finite difference method is used to solve the LLG equation. In such an approach, the entire sample is discretized into a rectangular mesh of size $\Delta_x \times \Delta_y \times \Delta_z$ whose lengths are comparable to the characteristic exchange length of the material defined as $\lambda = \sqrt{\frac{2A}{\mu_0 M_s^2}}$. The effective field (Equation 2.7) for each domain is computed considering all the major energy contributions (Equation 2.6), and the dynamics of magnetization in each domain is given by solving the LLG equation (Equation 2.4). In micromagnetics, we assume the magnetization in each domain to be the value at the center. With such an approximation, the anisotropy, Zeeman and demagnetization fields have a second order approximation $O(\Delta^2)$ where Δ is the cell dimension. The boundary condition can only affect the higher order terms and as such has no effect on the $O(\Delta^2)$ terms (anisotropy, Zeeman and demagnetization). The exchange field can be computed to a second or higher order accuracy. As such, the boundary conditions become important for exchange field computation. Generally, Neumann boundary condition $\frac{\partial \vec{m}}{\partial \hat{n}} = 0$ is used where $\hat{n}$ is the unit vector normal to the boundary. It is however seen that this boundary condition is not critical for second order exchange computation. For higher accuracy, Dirichlet boundary condition can also be used.

2.1.4 Spin Wave Dispersion

Like a typical wave traveling through a medium, spin waves are characterized by a dispersion relation that relates the frequency ω of the wave to the wavelength λ or wave-vector k. The characteristic or dispersion relation of the spin wave is, in general, defined by two types of interaction among the electron spins:

Long-ranged magnetic dipolar interactions

The long-wavelength spin waves, called dipolar or magnetostatic waves (MSWs), are characterized by the long range dipole-dipole interaction. Due to the inherent anisotropy of the dipolar interaction, the MSWs can be further classified depending on the relative orientation of the spin-wave wavevector k and the saturation magnetization M_S. In an in-plane magnetized film, waves propagating along and transverse to M_S are called *"backward volume magnetostatic waves (BVMSWs)"* and *"magnetostatic surface waves (MSSWs, also known as Damon-Eshbach waves)"*, respectively. Dipolar waves in a normally (out-of-plane) magnetized film are called *"forward volume magnetostatic waves (FVMSWs)"*.

Short-ranged exchange interactions

The short-wavelength spin waves, called exchange waves, are characterized by the short ranged interaction among the neighboring spins. Typically their wavelengths are less than 1 μm and are preferred for nanoscale devices.

A generalized theory of dipole-exchange spin wave have been put forward by Kalinikos and Slavin [72] where the the tensorial Greens function technique has been used to formulate the dispersion relation (see appendix B for details about the calculation). For thin out-of-plane magnetized film with perpendicular magnetic anisotropy (PMA) which will be the subject of the discussion in this chapter, spin waves exhibit the following dispersion

relationship

$$\omega^2 = \gamma^2 \Big[H_{PMA} + Ak^2 \Big] \Big[H_{PMA} + Ak^2 + M_S \Big(1 - \frac{1 - e^{-kd}}{kd} \Big) \Big] \tag{2.10}$$

where H_{PMA} is the effective out-of-plane internal magnet field accounting for externally bias magnet field, PMA and demagnetizing field. The above relation can be obtained from the generalized dispersion relation (Equation B.4) mentioned in appendix B.

2.1.5 Spin Waves for Beyond-CMOS Logic

For several decades, theoretical and experimental investigations have been carried out to unravel the fundamental physics of the spin waves. The recent years have however seen an active interest from the device and engineering community to utilize spin waves for information transmission and processing. This is due to several advantages provided by spin waves: (i) Joule-heat-free transmission of information without involving any charge transfer, (ii) superposition of spin waves providing ability to perform logical operations, (iii) no stand-by power requirement, and (iv) interaction between the spin wave bus and other devices being accomplished via magnetic coupling. The idea of magnon-based data processing has been put forward exploiting the wave nature of magnons. Encoding binary data in the amplitude of the spin wave and using a MachZehnder interferometer, Schneider et al. [73] and Li et al. [74] proposed spin wave logic gates. Recently, all-magnon based circuits namely spin-wave multiplexer [75] and magnon transistor in which the source-to-drain magnon current is controlled by the injection of magnons into the transistors gate [76] have been proposed for all magnon data processing[3]. However, as highlight in Section 1.5, focusing on developing logic devices that act as simple switches undermines the expressive power of these novel devices. The idea of non-conventional ways of computing using spin wave majority logic has been explored by Khitun and colleagues [59, 78–80]. The recent

[3] A comprehensive overview of *"magnonic spintronics"* can be found in the review article by Chumak et al. [77]

advances in voltage-controlled magnetoelectric (ME) devices, which can switch the magnetization with reduced energy dissipation compared to current-controlled devices, have provided an alternative pathway for excitation and detection of spin waves compared to inductive [81–83] or spin-torque [84, 85]. The scheme of ME excitation/detection of spin waves have been introduced in some previous works by Khitun and colleagues [79, 86, 87]; however, several issues remained unresolved causing major road-block in the further progress of spin wave logic.

2.1.6 Prior Work and Challenges

There are many requirements that any novel computing platform must meet before it can be adopted for use in real circuits and even before major investments in research and development become justifiable. Designing of a complete spin wave device (SWD) would require satisfying the five essential requirements for logic application: nonlinearity, amplification, concatenability, feedback prevention, and complete set of Boolean operations. Additionally, any practical realization of an all-magnon based computing system must undergo the essential steps of a careful selection of materials and demonstrate robustness with respect to thermal noise or variability. The scheme of ME excitation/detection of spin waves have been introduced in some previous works [79, 86, 87]. It is well-known that spin waves can cause small fluctuations of the magnetization around the equilibrium condition. Hence, spin waves on their own can not provide enough energy to the magnet to cross the barrier and switch from one in-plane stable state to the other. Khitun. et. al. introduced the concept of storing magnetic bits as canted magnetization states ($\sim 5^o$) of a ME cell and a propagating spin wave can switch the canted magnetization from one state to the other [79]. However, such small canted magnetic state would be vulnerable to thermal fluctuation resulting in loss of non-volatility, an attractive feature of spintronics. Furthermore, the essential characteristics like non-reciprocity (controlling the direction of signal flow such that the output gets affected by the input and not the reverse) and concatenability (cascad-

ing multiple logic gates) remained missing or lacked careful investigation in the previous works. A major drawback of the spin waves is the exponential decay of the signal amplitude. Hence, the realization of a feasible long multi-staged spin wave based circuitry would require either spin wave amplifiers to boost the signal amplitude [86] or convert spin wave signal to voltage signal at the end of each stage. A novel route for voltage-controlled parametric excitation and amplification of spin wave was introduced by Verba et. al. [88, 89] relying on voltage-controlled magentic anisotropy (VCMA). However, none of the prior works satisfied all the essential requirements for logic application mentioned earlier.

2.1.7 Overview of Chapter

In this chapter, the basic building blocks have been introduced in Section 2.2 along with the identification of suitable materials that can enable the experimental implementation of the developed ideas that follow. Section 2.3 delineates a novel scheme of full 180° switching of the magnetization by the propagating spin wave, realized by introducing a meta-stable magnetization state via the ME effect. Although spin waves can not provide enough energy for the magnet to cross the energy barrier, one can imagine a case where the ME effect can modify the energy profile of the magnet, making it go to a meta-stable out-of-plane state (90° switching) and once the ME effect is removed, the phase of the propagating spin waves can deterministically make the magnet go to either one of the stable in-plane configurations (another 90° switch). Thus, this scheme provides a more stable non-volatile memory element even when the effect of thermal noise is considered (see Section 2.6). The promising attribute of non-volatility for magnetic devices allows zero-static power dissipation [90–93] and enables implementation of logic-in-memory architectures [94–96]. The 90° switching of magnetization from a stable in-plane to a meta-stable out-of-plane state via ME effect is used to re-create new spin waves for transmitting signal to the next stage. This mechanism ensures an automatic amplification of spin wave signal at the end of each stage. Concatenability is ensured by designing the input and output of each stage in a

similar fashion such that the output of one stage can serve as the input of the next stage. The bistability of the ME cell magnet storing the information provides the non-linearity for logic application. In Section 2.4, a novel clocking scheme has been introduced which takes care of non-reciprocity while ensuring sequential detection, storage and transmission of information from one stage to the next stage in a cascaded SWD as explained in Section 2.5. As will be discussed later, the appropriate choice of the clock period results in the device acting as a buffer (PASS gate) or an inverter (NOT gate). This serves as a building block for performing wave-based computing as explained in details in Chapter 3. The proposed device thus ensures all the essential requirements for logic application: non-linearity, amplification, concatenation, feedback prevention, complete set of Boolean operations and robustness with respect to thermal noise and variability.

2.2 Building Blocks

Based of the general model described earlier for any beyond-CMOS device, two basic building blocks have been identified in this work: (a) a fundamental computing block that enables transmission (write data), detection (read data) and non-volatile storage (memory), and (b) a magnetic channel that supports spin wave propagation for transmission of information between the input and output. Figure 2.4(a) shows the general schematic of a spin wave logic.

2.2.1 Spin Wave Bus

In a spin wave logic, the channel that acts as a conduit for information transmission is often referred to as a spin wave bus (SWB). Traditionally, SWBs have been fabricated in the form of in-plane magnetized narrow magnetic stripes with commonly used materials like permalloy ($Ni_{81}Fe_{19}$) [97] and yttrium-iron-garnet YIG ($Y_3Fe_5O_{12}$) [98, 99] that provide low gilbert damping α. However, recent works on spin waves have highlighted the preference of using an out-of-plane magnetized over in-plane magnetized SWB owing to

several advantages. Firstly, it is possible to overcome the limitations of broken translational symmetry and anisotropic dispersion relation of backward volume spin waves that give rise to scattering processes where the waves interfere [100]. Secondly, it is possible to locally control the internal magnetic field via application of voltage controlled magnetic anisotropy (VCMA) [88]. While several experimental works have used a few hundred milli-Tesla (mT) of magnetic field for out-of-plane biasing, the usage of such an external magnetic field is incompatible with integrated device and circuitry. Multilayers like [Co/Ni] are be a potential candidates that can offer a bias-free out-of-plane magnetic configuration because of their inherent interface anisotropy arising from the spin-orbit interaction at the interface [101–105] and sustain a propagating spin wave [106, 107] via their low damping [108–111]. Hence, multilayers of [Co/Ni] with perpendicular magnetic anisotropy (PMA) are chosen as a convenient and well-studied material example for SWB (see Figure 2.4(b)). Note that the aim is to obtain a low PMA to minimize spin wave attenuation. Using a phenomenological treatment along with experimentally determined parameters [101–105], the effective PMA is calculated to be K_{eff} = 0.4 MJ/m^3 for a [Co(0.4 nm)/Ni(0.8 nm)]$_{10}$ multilayer. Detailed calculations are provided in Appendix A. Table 2.1 lists the material parameters considered in our simulation. Although idealized multilayers have been considered in the simulations characterized by low Gilbert damping as has been experimentally reported [109, 110], the extrinsic damping or de-phasing arising from sources like two-magnon scattering due to sample-inhomogeneity and spin pumping at the heavy metal/ferromagnet interface can give rise to additional spin wave damping. Perpendicularly magnetized YIG and Heusler alloy ($Co_2Fe_{0.4}Mn_{0.6}Si$) exhibiting low magnetic damping [112, 113] may provide an attractive alternative for low-loss spin wave channel.

2.2.2 Magnetoelectric Cell for Excitation/Detection

Traditionally, nano or microscale antennas are used to excite spin waves and the detection is done via inductive voltage produced by the propagating spin waves [78, 82, 83, 114].

Table 2.1: Material parameters of SWB $[Co(0.4\ nm)/Ni(0.8\ nm)]_{10}$

Parameter	Value	Units
Length	100	nm
Width	40	nm
Thickness	12[*], 8-15 [#]	nm
Saturation magnetization M_s	790	kA/m
Exchange constant A_{exch}	16	pJ/m
Gilbert damping constant	0.01	-
Out-of-plane anisotropy H_K	16.78	kA/mm
Out-of-plane anisotropy K_{SWB}	4	MJ/m^3

[*] For built-in strain, see Section 2.6.2
[#] For exchnage-spring, see Section 2.6.3

However, such a scheme suffers from high-power dissipation. A more energy efficient way to excite spin waves is to use the magnetoelectric (ME) effect in single phase or composite multiferroics materials. The ME effect, described as the coupling between the magnetic and the electric properties of a material, has been the focus of active research lately owing to their potential application in low-power non-volatile memory and logic [50, 115]. Single-phase multiferroics are rare, have small magnetoelectric coefficients[4] (10^{-9}-10^{-12} s/m), or have issues with low cycle numbers [116]. The largest and most robust magnetoelectric effects (10^{-5}-10^{-7} s/m) have been demonstrated in composite magnetoelectrics [117, 118]. Recent works on the ME effect in composite multiferroics [119, 120] have shown that in a heterostructure consisting of a ferroelectric (FE) or piezoelectric (PZ) material sandwiched between two metal electrodes and a top magnetostrictive ferromagnetic material, the energy landscape of a top magnet can be modified by applying a voltage across the thickness of the ferroelectric or piezoelectric layer. Such a heterostructure, referred to as a magnetoelectric cell or ME cell, has been proposed in some earlier works [79, 87] and will be utilized here as the most fundamental computing block of a magnonic logic, performing the tasks of spin wave generation/transmission, detection and also serving as a non-volatile memory element

[4]Magnetoelectric coupling coefficient $\alpha = \mu_0 \Delta M / \Delta E$ dictates the efficiency of an applied electric field to be transduced into a magnetization change and thus governs the energy consumption for the electric field control of magnetism in these materials

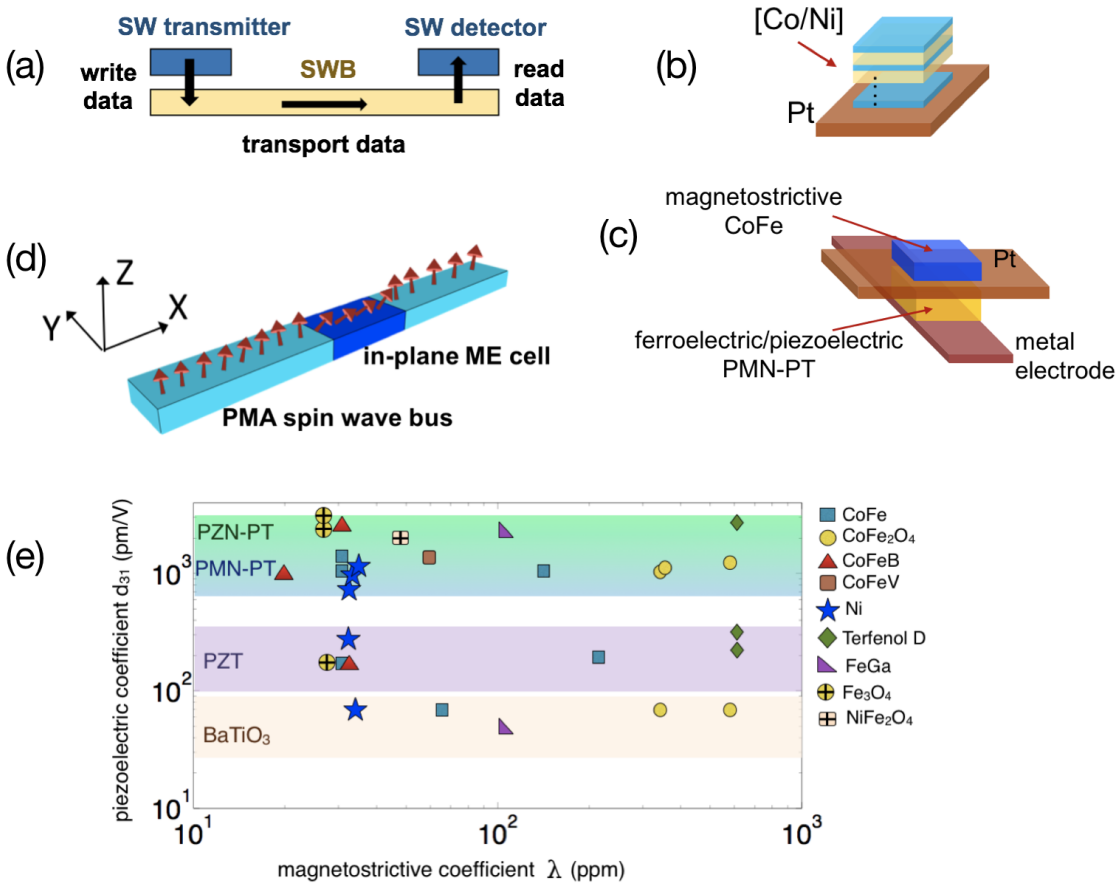

Figure 2.4: (a) Gerenal schematic of a spin wave logic device consisting of a spin wave transmitter (for writing data), detector (for reading data) and spin wave channel (for transmitting data). The basic building blocks considered in this work are (b) PMA $[Co(0.4)/Ni(0.8)]_{10}$ multilayer spin wave bus and (c) ME cell comprising of a magnetostrictive $Co_{60}Fe_{40}$ layer grown on (001) PMN-PT ferroelectric layer. (d) Micromagnetic picture of mutually orthogonal spin configuration of PMA SWB and normally in-plane magnetized ME cell. (e) Map of the magnetostrictive coefficient λ of the magnetic layer and piezoelectric coefficient d_{31} of the piezoelectric/ferroelectric layer along with their compatibility for some of the demonstrated stacks.

[57] (see Figure 2.4(c)). With ultra-low power dissipation being the ultimate goal in mind, the target piezoelectric material must possess a high piezoelectric coeffcient (d_{31}) while the magnetic layer must display a high magnetostrictive coeffcient (λ) simultaneously. Figure 2.4(d) shows an illustration of mutually orthogonal spin configuration of PMA SWB and normally in-plane magnetized ME cell, representing the ground state of the ME cell-SWB structure.

Table 2.2: Material parameters of ME cell $Co_{60}Fe_{40}$

Parameter	Value	Units
Length	80	nm
Width	40	nm
Thickness	12	nm
Saturation magnetization M_s	800	kA/m
Exchange constant A_{exch}	20	pJ/m
Gilbert damping constant	0.027	-
Magnetostriction coefficient λ	200	ppm
Young's modulus Y	200	GPa

Choice of magnetostrictive magnetic material

Figure 2.4(e) shows a comprehensive map of the piezoelectric and magnetostrictive coefficients for a wide range of material including their compatibility[5]. Nickel (Ni) [122, 123] has been extensively used experimentally to demonstrate magnetoelectric effect, however it displays a low magnetostrictive coefficient ($\lambda \sim$ -32 ppm). $CoFe_2O_4$ [124] offers an order of magnitude improved λ, however it may provide a lower thermal stability/reliability owing to low saturation magnetization. Similar high magnetostriction of λ = 150 ppm has been reported in equiatomic composition of $Co_{0.5}Fe_{0.5}$ [125, 126]. Recent work by Hunter et. al. [127] has reported an enhancement of magnetostriction at the (fcc+bcc)/bcc phase boundary with effective λ as high as 260 ppm. Alternative materials include low magnetostrictive CoFeB [128], CoFeV [129], Fe_3O_4 [130], $NiFe_2O_4$ [131] and high magnetostrictive $Fe_{0.8}Ga_{0.2}$ [132] ($\lambda > 250$ ppm) and highest magnetostriciton observed in $Tb_xDy_{1-x}Fe_2$ [133]. In this chapter, $Co_{0.6}Fe_{0.4}$ has been considered as the choice of magnetostrictive material with λ = 200 ppm. An added advantage of this choice is a much more mature fabrication process for CoFe compared with that of Terfenol-D. Table 2.2 lists all the material parameters of the magnetostriction ferromagnetic layer considered in our simulation.

[5] A comprehensive reference list of the materials discussed next can be found in ref. [121]

Table 2.3: Material parameters of Piezoelectric (001)PMN-PT]

Parameter	Value	Units
Length	$>$80	nm
Width	$>$40	nm
Thickness	30	nm
Piezoelectric coefficient d_{31}	-1000	pV/m

Choice of piezoelectric material

In contrast to polycrystalline materials like Pb(Zr,Ti)O_3 (PZT), relaxor based ferroelectric single crystals like (Pb($Zn_{1/3}Nb_{2/3}$)O_3)-[$PbTiO_3$] (PZN-PT) and (Pb($Mg_{1/3}Nb_{2/3}$)O_3)-[$PbTiO_3$](PMN-PT) do not require morphotropic phase boundary conditions for exhibiting ultrahigh piezoelectric strain. $<$001$>$ oriented relaxor based rhombohedral crystals such as (1-x)PZN-PT ($x < 9\ \%$) and (1-x)PMN-PT ($x < 35\ \%$) are known to demonstrate ultrahigh piezoelectric coefficient d_{33} and strains of 0.6 $\%$-0.8 $\%$ with applied electric fields less than the dielectric breakdown limit [134]. The reason for such high strain is presumed to be associated with an electric field induced rhombohedral-tetragonal phase transition. In this work, (001) PMN-PT has been considered. The material parameters used in the simulations are highlighted in Table 2.3. Substrate induced clamping can drastically reduce the piezoelectric response of thin ferroelectric films from their bulk value. As such the thickness of the PMN-PT film has been assumed to be atleast greater than 30-50 nm. The lateral size of the PMN-PT film has also been assumed to be larger than the thickness to allow the formation of an in-plane isotropic biaxial strain instead of anisotropic strain [135]. It has been demonstrated that a high strain relaxation of upto 90$\%$ can occur in thick ferroelectric films (thickness $>$ lateral dimensions) [135]. As such the thickness of the CoFe layer of the ME cell has been limited to around 12 nm. The comparison in Figure 2.4(e) shows that, with the chosen combination of piezoelectric PMN-PT and the ferromagnet CoFe, one can reach a high product of coupling coefficient.

2.3 Device Operation

Figure 2.5(a) shows a single stage spin wave logic device consisting of a ME spin wave transmitter and a detector connected via a SWB. The working principle of the ME cell is based on the magnetoelectric effect, specifically voltage-controlled strain-mediated magnetization switching. Under nominal condition (zero applied voltage) the magnetization of the ME cell stays in-plane storing either a logic "1" or "0". Bit "1" and "0" are designated to the magnetization states pointing in the +$\hat{x}$ or -$\hat{x}$ direction, respectively. As shown in Figure 2.5(b), applying an out-of-plane electric field E_z across the thickness of a (001) oriented ferroelectric or piezoelectric layer (poled in the perpendicular direction and having in-plane isotropic properties) causes an in-plane biaxial strain

$$\epsilon_{xx} = \epsilon_{yy} = \epsilon_s = \epsilon_{res} + d_{31}E_z \tag{2.11}$$

that gets coupled to the overlaying ferromagnetic layer through the interface and thin Pt electrode, where ϵ_{res} represents built-in strain and d_{31} represents the piezoelectric coefficients. A simplistic model [136, 137] assumes the generation of uniform strain within the FE that gets fully coupled to the top magnetostrictive magnetic layer (100% coupling efficiency). The magenetoelastic energy E_{ME} describing the coupling between the magnetization and the strain is given by

$$\begin{aligned} E_{ME} &= B_1\Big[\big(m_x^2 - \frac{1}{3}\big)\epsilon_{xx} + \big(m_y^2 - \frac{1}{3}\big)\epsilon_{yy} + \big(m_z^2 - \frac{1}{3}\big)\epsilon_{zz}\Big] \\ &\quad + B_2\big(m_x m_y \epsilon_{xy} + m_y m_z \epsilon_{yz} + m_z m_x \epsilon_{zx}\big) \end{aligned} \tag{2.12}$$

where B_1 and B_2 are the magnetoelastic coupling coefficients, m_i (i=x, y, z) are the direction cosines of magnetization $\vec{M}$, and ϵ_{xx}, ϵ_{yy} and ϵ_{zz} are the elastic strains defined in the crystallographic reference frame (same as the principal crystal axes for (001)-oriented epitaxial systems). B_1 and B_2 can be further described in terms of the magnetostrictive

constants, λ_{100} and λ_{111} of the FM films [138] such that

$$B_1 = -\frac{3}{2}\lambda_{100}\big(c_{11} - c_{12}\big); \quad B_2 = -3\lambda_{111}c_{44} \tag{2.13}$$

For epitaxial films and for polycrystalline films $\lambda_{100} = \lambda_{111} = \lambda_s$. The elastic constants of the FM are defined by c_{11}, c_{12}, and c_{44}, respectively. To a first order approximation, the energy expression can be further reduced in our condition to

$$E_{ME} = -\frac{3}{2}\lambda Y\bigg[\big(m_x^2 - \frac{1}{3}\big)\epsilon_{xx} + \big(m_y^2 - \frac{1}{3}\big)\epsilon_{yy}\bigg] = \frac{3}{2}\lambda Y\epsilon_s\big(m_z^2 - \frac{1}{3}\big) \tag{2.14}$$

and gives rise to an equivalent out-of-plane strain-induced anisotropy calculated as

$$K = \frac{3}{2}\lambda Y\epsilon_s = \frac{3}{2}\lambda Y(\epsilon_{res} + d_{31}E_z) = \frac{3}{2}\lambda Y(\epsilon_{res} + d_{31}\frac{V}{t_{PE}}) \tag{2.15}$$

where V is the voltage applied across the thickness t_{PE} of the piezoelectric layer. An up to 90^o magnetic easy axis rotation can be achieved as the isotropic in-plane strain surpasses a critical limit of shape anisotropy $E_{shape} = \frac{1}{2}\mu_0 M_s^2$ causing a voltage-induced strain-mediated out-of-plane anisotropy and subsequently magnetization switching. Such in-plane to out-of-plane magnetization switching dynamics can be used to excite spin waves.

The clocking sequence for the two ME cells and the working principle, based on voltage-controlled strain-mediated magnetization switching, are illustrated in Figures 2.5(c) and (d), respectively. Before transmitting information from the transmitter to the detector, first a voltage is applied to the detector ME cell through clock 2 which causes the detector to switch out-of-plane while the transmitter ME cell stays in-plane storing either a logic "1" or "0". Then, a voltage is applied to the transmitter ME cell through clock 1, causing it to switch from in-plane to out-of-plane configuration and in the process exciting spin waves with the information encoded into the phase of the waves. A +$\hat{x}$ to +$\hat{z}$ magnetization switching creates a spin wave with "0" phase, while a -$\hat{x}$ to +$\hat{z}$ switching creates spin waves

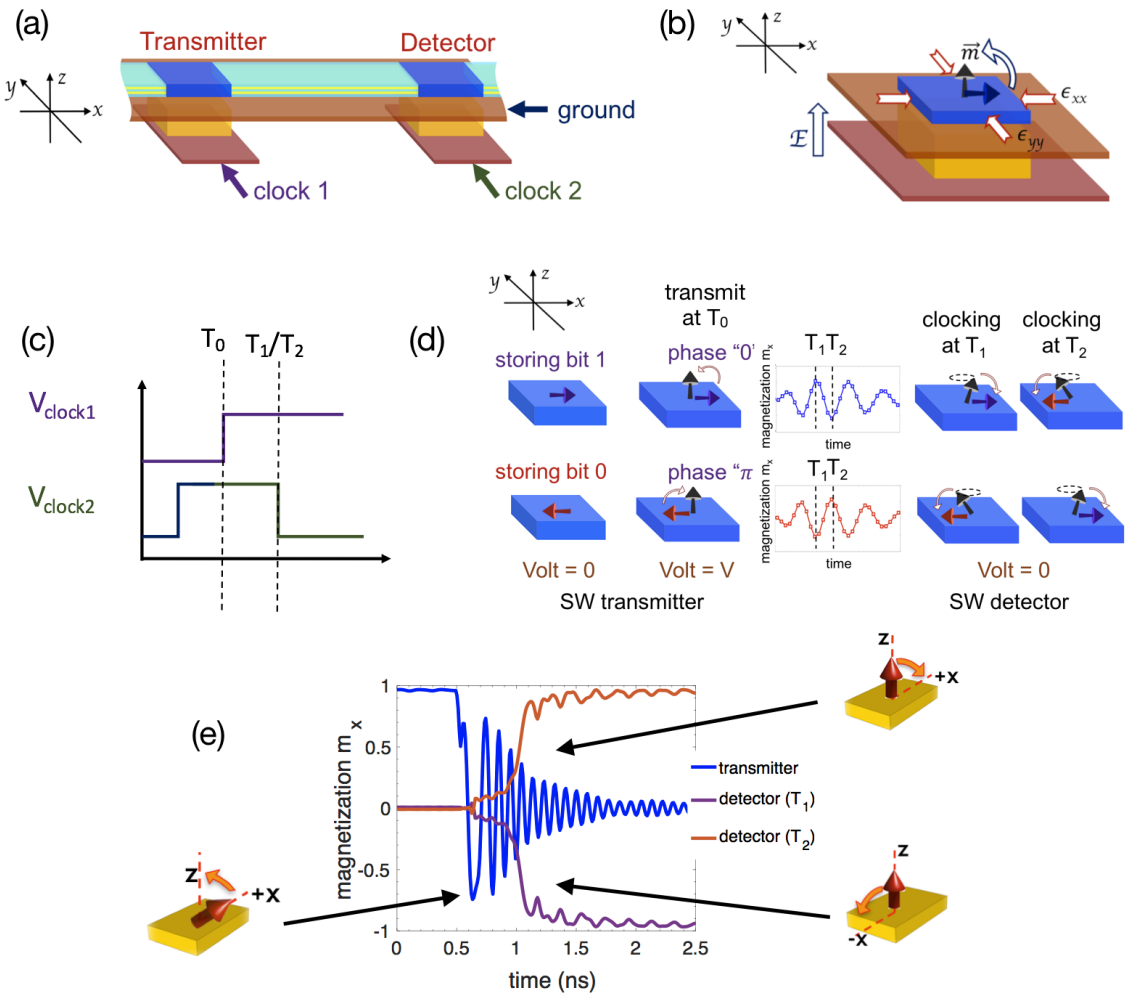

Figure 2.5: (a) Illustration of a single stage spin wave logic device, (b) Schematic of magnetostriction-assited switching of the ME cell, (c) Clocking scheme for the spin wave logic device, (d) Working principle of the spin wave device, based on voltage-controlled strain-mediated magnetization switching, (e) Magnetization of the transmitter and detector ME cell

with opposite "π" phase. The excited spin wave travel through the SWB to the detector and upon arrival, the voltage of the detector ME cell is switched off causing a phase-dependent out-of-plane to in-plane magnetization switching. Interestingly, depending on the time the voltage is switched off, i.e., either T_1 or T_2 as shown in Figure 2.5(d), we end up detecting different phase of the wave and the detector ME cells magnetization falling either in the +$\hat{x}$ or -$\hat{x}$ direction as shown in Figure 2.5(e). In other words, the logic function of the SW device (buffer or inverter) can be defined simply by choosing the appropriate time of

clocking. From here on, the time when the voltage of the detector ME cell is switched off will be referred to as the *clocking time*. The clocking time is set equal to the per stage propagation delay of the spin wave signal [57]. This scheme is in contrast to prior work on magnonic logic that relies on the length of the interconnect compared to the wavelength of the spin wave [78] and offers the possibility of having magnonic reconfigurable logic. The proposed device concept is universal in the sense that alternative mechanisms for 90^o magnetization switching like VCMA can also be used instead of magnetostriction.

2.4 Clocking

The non-reciprocity and the sequential transmission of information from one stage to the next in a SWD is taken care of by introducing a novel clocking scheme shown in Figure 2.6(a) for a 3-stage cascaded SWD. External CMOS circuitry can be designed to generate the clocking signals that toggle between the ground and supply voltage, and have a clock skew between each other; clocking circuitry have been discussed later in Section 2.7. ME cells are designed as edge-triggered elements that transmit and receive signals at the rising and falling edges of the clock. The rising edge of the clock represents the excitation of spin waves for information transmission while the falling edge represents the detection and storage of signal. Note that both the rising and falling edges of the clock (magnetization going in-plane to out-of-plane or vice versa) excite spin waves that can travel in both the forward and backward directions. Figure 2.6(b) shows the magnetization dynamics of the 3 cascaded ME cells.

The basic operating principle of the clocking scheme is shown in Figure 2.6(c). At time $t = t_1$ when ME cell 2 excites spin waves by switching from in-plane to out-of-plane, the previous stage ME cell 1 maintains an in-plane stable configuration. Since the spin waves propagating in the PMA SWB are in reality only the precessional rotation of the out-of-plane magnetization, having an in-plane magnetization of ME 1 blocks the back-propagating waves as well as does not affect the state of ME 1 as seen at time $t = t_2$.

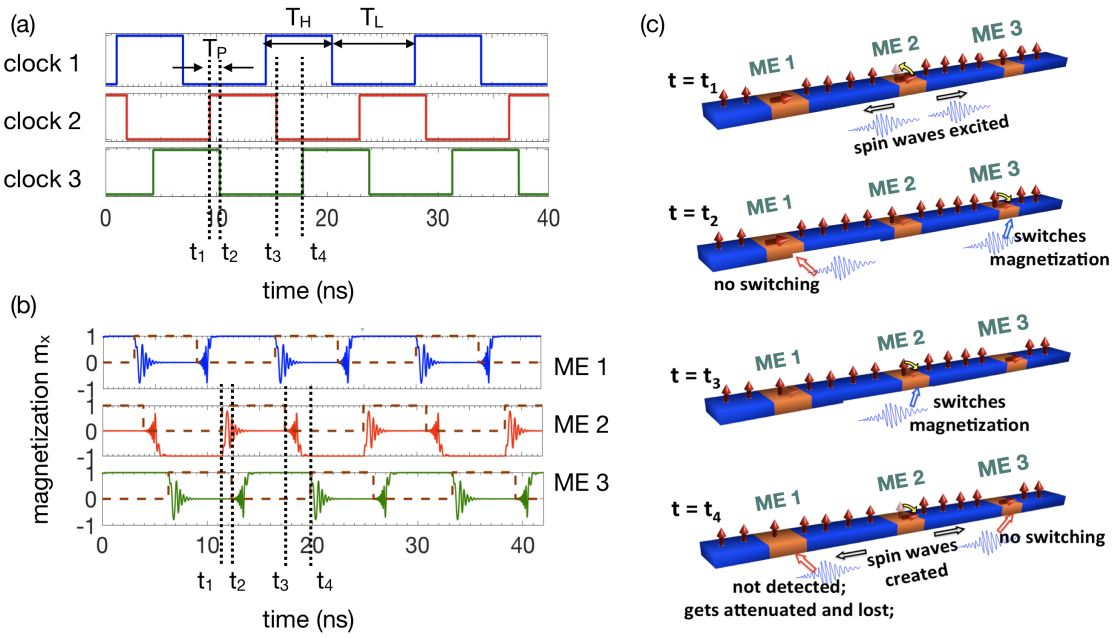

Figure 2.6: (a) The proposed clocking scheme which enables a sequential transmission of information and non-reciprocity. The rising edge of the clock represents the excitation of spin waves while the falling edge represents the detection and storage of signal. T_P denotes the propagation delay of the spin waves from one ME cell to the next while T_H and T_L represents the time a clock stays high or low. (b) Shows the corresponding magnetization dynamics of the ME cells. (c) Illustration of the working of the clocking scheme showing a pictorial representation of the spatial variation of the magnetization at different snapshots of time.

On the other hand, the next stage ME cell 3 is maintained in an out-of-plane meta-stable condition by applying a voltage, waiting for the spin waves to arrive and being detected. As soon as the waves reach ME 3 at time $t = t_2$, the voltage on ME 3 is removed allowing the magnetization to go in-plane. The switching direction ($\pm\hat{x}$) is dictated by the phase of the incoming waves (0 or π).

At time $t = t_3$ when ME 2 detects spin waves, ME 3 maintains an in-plane stable state thus blocking the forward propagating spin waves created during detection by ME 2. Since ME 1 has to be maintained in an out-of-plane meta-stable state in order to detect the spin waves that would be created by the stage previous to ME 1, the backward propagating spin waves from ME 2 pass through ME 1 without getting detected. Eventually, the waves get attenuated and are lost.

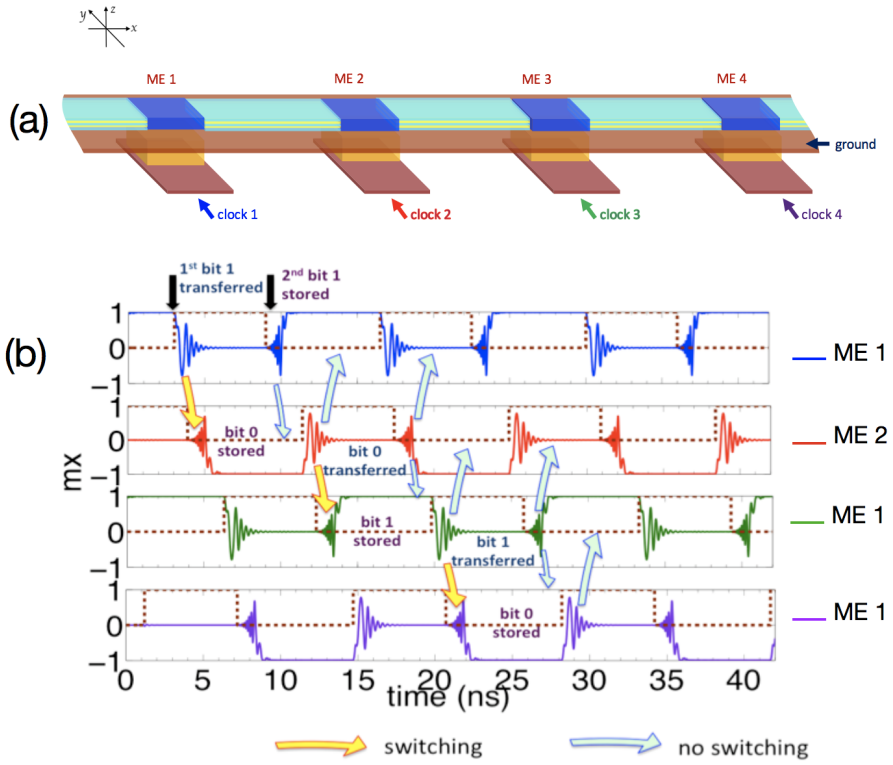

Figure 2.7: Sequential transmission of information in a clocked four-stage cascaded SWD that acts as a chain of inverters shown in (a). Figure (b) shows the transmission of a train of bit "1". The yellow arrows indicate the case when the spin waves propagate and switch the next stage ME cell while the blue arrows indicate the case when the propagating spin waves do not affect the dynamics of the other ME cells.

The delay between the rising edge of one clock and the falling edge of the next clock $(t_1 - t_2)$ is equal to the propagation delay T_P of the spin waves from one ME cell to the next and has to be carefully sized for designing the clocking scheme. The presence of the delay T_P and the requirements for non-reciprocity leads to a negative clock skew and the need for having multiple clocks. Further details about choosing the high time T_H and the low time T_L for the clocking scheme can be found in [57].

2.5 Sequential Transmission of Information - Pipelining

Next, the clocking scheme is applied to a four-stage cascaded structure as shown in Figure 2.7(a)) to investigate sequential transmission of information. By appropriate choice of

T_P, one can ensure that the structure acts as a chain of inverters. Three cases have been explored here: (a) transmitting all bit "1"s, (b) transmitting all bit "0"s, and (c) transmitting alternately bit "1"s and "0"s. Figure 2.7(b) shows the result of numerical simulation for transmitting a train of bit "1". We assume the first ME cell 1 is initially storing a bit "1". As the clock 1 goes high, the magnetization goes out-of-plane creating spin waves and transmitting bit "1" (shown by yellow arrow). The next stage ME cell 2 is held in the out-of-plane state by applying voltage till the spin wave packet arrives. On arrival, clock 2 goes low and it's magnetization goes in-plane depending on the phase of the wave. We see the transmission of bit "1" successfully switches ME 2 to m_x = -1 final state thus storing bit "0". As the magnetization of the ME 1 goes in-plane (m_x = 1) storing the second bit "1", it creates spin waves which do not affect ME 2 which is in a stable in-plane configuration (shown by blue arrow). ME 2 continues to store bit "0" until clock 2 goes high creating spin waves. These waves propagate in both the directions but do not affect the previous stage ME cell 1 as it is in a stable in-plane configuration (shown by blue arrow). The forward propagating spin waves transmit bit "0" to ME 3 (shown by yellow arrow). This mechanism goes on thus detecting, storing and transmitting train of bits from one stage to the next. Figures 2.8(a) and 2.8(b) show the transmission of a train of bit "0" and alternating bit "1" and "0" respectively in a similar fashion. A similar concept applies to the design of a chain of buffers where a bit "1" gets stored as a bit "1" in the next stage and vice-versa.

2.6 Thermal Reliability

Thermal noise has constantly plagued the field of spintronics, influencing magnetic retention, read and write failures. The dynamic variability introduced by thermal fluctuations poses a serious threat to the performance of spintronics logic and memory. The effect of thermal noise on spin wave logic is two-fold: (a) introduction of phase noise by randomizing the amplitude and phase of the propagating spin wave, and (b) affecting the trajectory of the magnetization dynamics of the ME cell during the course of spin wave excitation

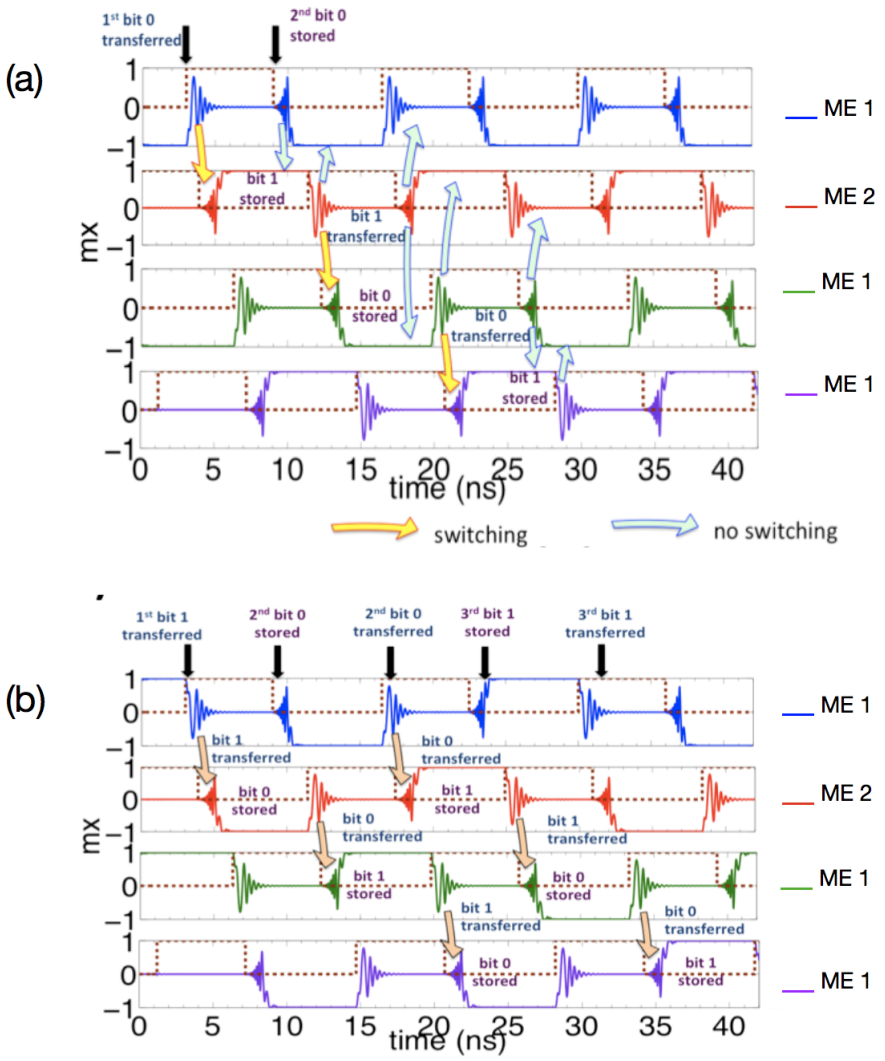

Figure 2.8: Figures (a) and (b) show the transmission of a train of bit "0" and alternate bits "1" and "0", respectively. The yellow arrows indicate the case when the spin waves propagate and switch the next stage ME cell while the blue arrows indicate the case when the propagating spin waves do not affect the dynamics of the other ME cells.

and detection. The effect is seen to be most crucial during the course of detection. Firstly, the amplitude ($\theta = cos^{-1}m_z$) and phase ($\phi = tan^{-1}(m_y/m_x)$) of the arriving spin wave, detected at the falling edge of the clock displays a Gaussian distribution around the mean value expected without any thermal noise as shown in Figures 2.9(a) and (b). Figure 2.9(b,i) shows the case of an error-free logic function acting as a buffer where the detected phase (ϕ) falls within the highlighted windows of deterministic switching. Hence, all the trans-

mitted bit "1"s are stored correctly and same for bit "0"s. On the contrary, Figure 2.9(b,ii) depicts a more erroneous case where the detected phase (ϕ) spreads over both the windows giving rise to a situation where some of the transmitted bit "1"s get detected as bit "0"s and so on. Also note that the white gap separating the regions of deterministic detection of bits "1"s and "0"s represents a non-deterministic situation as explained later.

Additionally, as the magnetization transitions from out-of-plane to in-plane configuration during the course of spin wave detection, it undertakes a highly precessional trajectory before relaxing to one of the energy minima states ($\pm$ x). Such a precessional trajectory is highly vulnerable to thermal noise and even a small variation can cause the switching to become non-deterministic. The reason for such a precessional trajectory can be understood by looking at the energy landscape and constant energy trajectories of the magnetization (see Figure 2.9(c)). In the absence of damping and thermal noise, the magnetization does precessional rotation in a conservative or constant energy trajectory which can be distinguished into two categories - high energy orbit around the out-of-plane hard axis (z), also called *"out-of-plane precession (OPP)"* and low energy orbit around the in-plane easy axis (x), also called *"in-plane precession (IPP)"*. The evolution of such trajectories can be described analytically by solving the LLG equation in the absence of damping and thermal noise [139, 140]. The energy landscape of the nano-magnet and a set of such constant energy trajectories are shown in Figure 2.9(c). Note the positions of the energy minima, saddle point (marked by **X**) and energy maxima, which are along the x ,y and z-axes respectively. Upon adding the contribution of damping, the dynamical evolution of the magnetization deviate from the constant energy trajectory and the closed orbit transforms into a finely spiraling trajectory approaching an energy minima as illustrated in Figure 2.9(c). The magnetization follows the constant energy trajectories fairly closely, drifting slowly from one higher energy trajectory to the next lower one, losing energy in the process via damping.

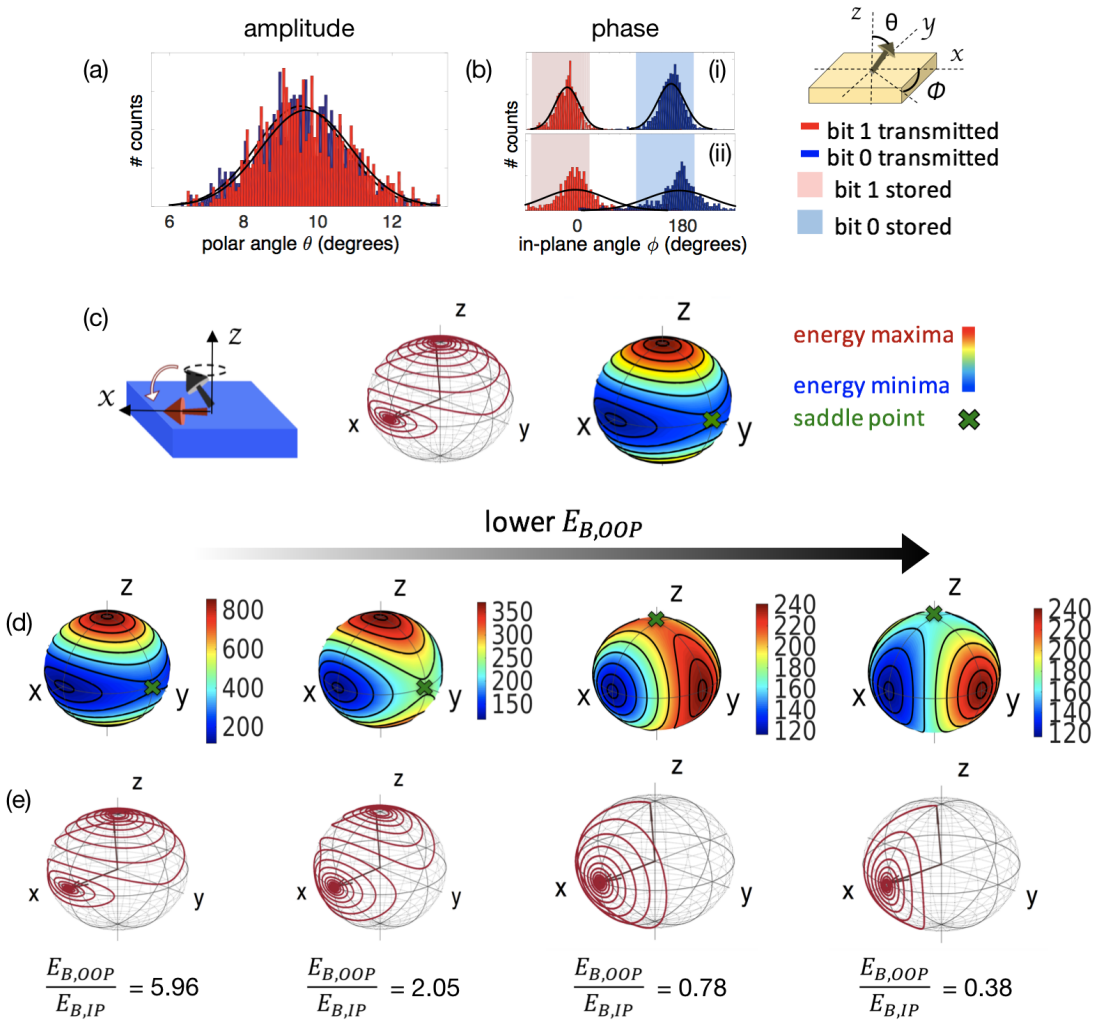

Figure 2.9: (a, b) Gaussian distribution of the amplitude ($\theta = cos^1 m_z$) and phase ($\phi = tan^1(m_y/m_x)$) of the arriving spin wave, detected at the falling edge of the clock, (c) Schematic of the dynamics of the ME cell during the course of SW detection, magnetization relaxation trajectory from out-of-plane to in-plane configuration and energy landscape of the nano-magnet. The colormap shows energy in k_BT. The black lines represent the constant energy trajectories in which the magnetization gyrates in the absence of damping and thermal noise, (d, e) Change in the energy landscape and the magnetization relaxation trajectory due to the lowering of the out-of-plane energy barrier $E_{B,OOP}$. The position of the energy maxima and the saddle point interchanges as $E_{B,OOP} < E_{B,IP}$.

2.6.1 Phase Dependent Deterministic Switching

One can, however, imagine a scenario where the energy landscape of the nano-magnet is modified by lowering the out-of-plane energy barrier $E_{B,OOP} = \frac{1}{2}\mu_0 M_s^2 (N_z - N_{cd} - N_x)V$

via introducing a small compensation in demagnetization N_{cd}. Here, M_s is the saturation magnetization, V is the volume and N_x, N_y and N_z are the demagnetization tensors under single-domain or macrospin assumption. This alters the constant energy orbits, lowering the number of *OPP*s and making more concentric *IPP*s around the energy minima (Figure 2.9(d)). Beyond a critical compensation, $E_{B,OOP}$ becomes lower than the in-plane energy barrier $E_{B,IP} = \frac{1}{2}\mu_0 M_s^2(N_y - N_x)V$, the saddle point shifts to the z-axis while the y-axis becomes the energy maxima. The energy landscape and a set of constant energy trajectories under this scenario is shown in Figure 2.9(d) for the cases of $E_{B,OOP}/E_{B,IP}$ = 0.78 and 0.38. Consequently, the dynamical evolution of the magnetization changes from a highly precessional one to a fairly damped one as shown in Figure 2.9(e). The cut down in the precessional trajectories makes the relaxation of the magnetization primarily dependent on the initial magnetization angle (θ and ϕ), with very little scope for the thermal fluctuations to alter the path of the magnetization and make the switching non-deterministic [141]. It must be noted that there are two constraints which limit the degree of compensation. Firstly, beyond a threshold value $N_{cd} = (N_z - N_x)$, $E_{B,OOP}$ becomes negative, denoting that the in-plane stable magnetization states ($\pm x$) are lost and the magnet becomes perpendicularly magnetized even in the absence of any ME effect. Secondly, the energy barrier $E_{B,OOP}$ decreases with the increase in compensation N_{cd} (see Figure 2.10(b)) and beyond a certain threshold, crosses the 40 k_BT mark, a minimum required for retaining any reasonable memory state lifetime.

First, a simple macro-spin model is used to demonstrate the impact of partially canceling the demagnetizing field on the deterministic switching of the magnet. An isolated nano-magnet in the shape of a cuboid with x, y and z being the in-plane easy axis, in-plane hard axis and out-of-plane hard axis respectively is analyzed using a simple macro-spin model. The scenario of spin wave detection, where the ME cell is allowed to relax from an out-of-plane metastable to an in-plane stable state with initial magnetization angles θ and ϕ provided by the spin wave, is mimicked by allowing the magnetization of the nano-

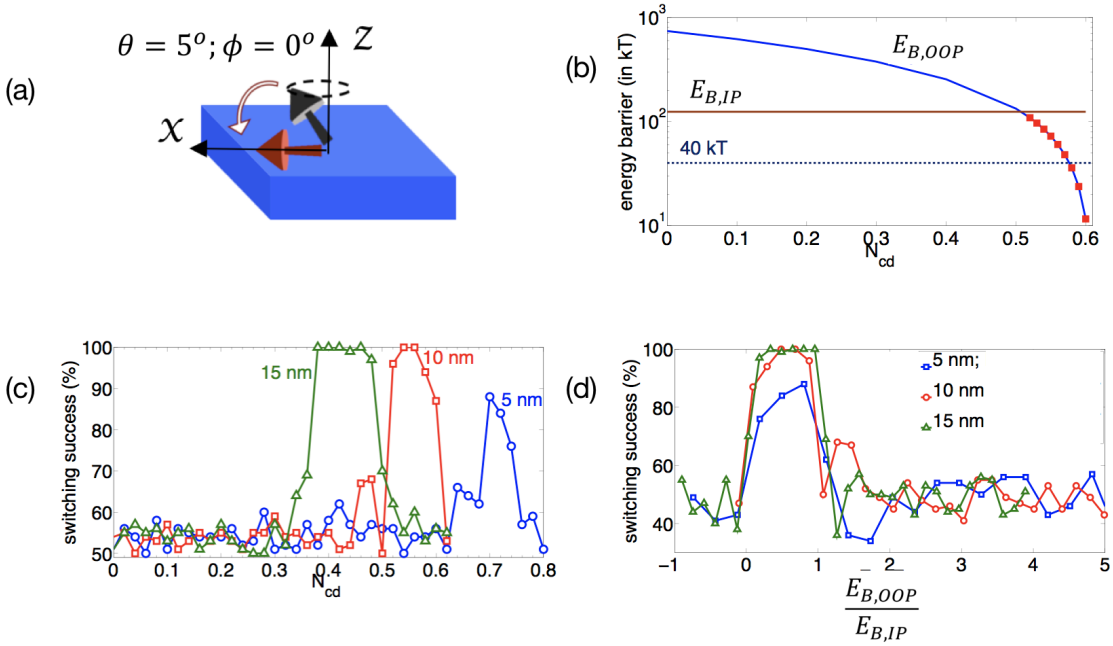

Figure 2.10: (a) Schematic of a single-domain where the scenario of SW detection has been mimicked by allowing the magnetization of the nano-magnet to fall in-plane from an initial out-of-plane state with fixed $\theta = 5°$ and $\phi = 0°$. (b) Lowering of $E_{B,OOP}$ less than $E_{B,IP}$ as the compensation N_{cd} is increases for a 10 nm thick nano-magnet. (c) Switching success of the nano-magnet as a function of compensation of demagnetization for 5, 10 and 15 nm thickness. The lateral dimensions are kept constant at 80 nm x 40nm. (d) Switching success as a function of the ratio of the energy barriers $E_{B,OOP}/E_{B,IP}$.

magnet to fall in-plane from an initial out-of-plane state with fixed $\theta = 5°$ and $\phi = 0°$ (see figure 2.10(a)). The choice for the initial angles is in close agreement with that provided by spin waves. Any fluctuations in the initial angles have been neglected since the focus here is only on the relaxation dynamics under thermal noise. To test for the impact of compensation of demagnetization on the switching success of the nano-magnet, numerical simulations have been performed by solving the stochastic LLG equation in the presence of thermal noise. In this example, nickel (Ni) has been used as the nano-magnet material and 100 simulations have been performed for each of the data points to capture the effect of thermal noise. With the initial magnetization angle fixed at $\theta = 5°$ and $\phi = 0°$, the switching success has been defined as the probability of the nano-magnet to fall into a preferred final magnetization state, which here is the $+\vec{x}$ direction. Figure 2.10 (c) shows the

remarkable impact of compensation of demagnetization on the switching success of the nano-magnet, paving the path for a more thermally reliable spin wave device. The sharply defined window where the switching success drastically increases can be obtained when the ratio $E_{B,OOP}/E_{B,IP} < 1$ as shown in Figure 2.10 (d) and is given by

$$\Delta \leq E_{B,OOP} \leq E_{B,IP} \tag{2.16}$$

$$N_z - N_y \leq N_{cd} \leq N_z - N_x - \frac{2\Delta}{\mu_0 M_s^2 V} \tag{2.17}$$

where $\Delta \sim 40 k_B T$. Note that for 5 nm thickness, even if the saddle point shifts to z axis under the condition $E_{B,OOP}/E_{B,IP} < 1$, the switching success is still low which maybe the result of a relatively low energy barrier $E_{B,OOP} \sim 40 k_B T$ (Figure 2.10(b)) or a relatively small volume of the nano-magnet.

The next question to answer is how to translate the theoretical idea of phase-dependent switching of the spin wave detector to a practical realization of a thermally reliable magnonic device. Here, two viable options have been investigated - (a) using the built-in strain in the ME cell for compensation of the demagnetization, and (b) using an exchange-spring structure which inherently modifies the energy landscape of the ME cell magnet as desired.

2.6.2 Built-in Strain

The first possible route is to take advantage of a *"built-in strain"* in the ME cell [121]. Figure 2.11(a) illustrates one possible layout of a spin wave logic circuit, with the main building blocks - ME cell and PMA SWB highlighted in Figure 2.11(b). Recent works on the growth and characterization of relaxor ferroelectric materials have demonstrated the possibility to engineer a desired built-in strain in a thin ferroelectric film grown epitaxially on an appropriate substrate. This misfit strain arising from the lattice mismatch and/or thermal expansion coeffcient mismatch between the film and the substrate can be as high as -0.42% for (001) $Pb(Zr_{1x}Ti_x)O_3$ (PZT) grown on $SrTiO_3$ (SRO) substrate [142] and -

0.46% for (001) 0.9(Pb($Mg_{1/3}Nb_{2/3}$)O_3) - 0.1[$PbTiO_3$] (0.9PMN 0.1PT) grown on (001) $LaAlO_3$ substrate [143]. The degree of in-plane misfit strain can be varied by using different substrates like (La,Sr) (Al,Ta)O_3 (LSAT), $SrTiO_3$ (STO) and MgO. Here, we consider the scenario of an epitaxially grown (001) PMN-PT on an appropriate substrate capable of producing a small built-in strain of -0.31% to -0.37%. The PMN-Pt layer is sandwiched between a bottom metallic electrode and a top thin layer of Pt. The Pt is assumed to be thin enough to allow an efficient strain transfer to the top magnetostrictive ferromagnetic layer of $Co_{60}Fe_{40}$.

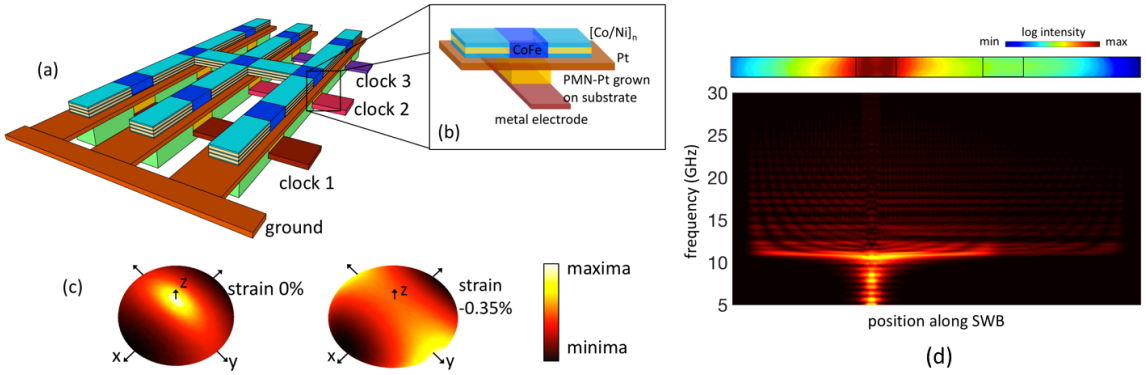

Figure 2.11: (a)Illustration of a possible layout of a spin wave logic circuit,(b)Details of the main building blocks - ME cell and PMA SWB. The ferroelectric PMN-PT is assumed to be epitaxially grown on an appropriate substrate in order to produce a small built-in strain. (c) Energy landscape of the CoFe layer of the ME cell under the case of 0 and -0.35 % built-in strain. (d) Spin wave transmission from the transmitter ME cell through the SWB to the detector ME cell and the frequency spectra along the length of the SWB, obtained from FFT of the x-component of the magnetization.

To better elucidate the impact of this built-in strain (ϵ_{res}) on the switching error, we first look at the energy landscapes of the ME cells magnetic layer under a zero ϵ_{res} condition and under ϵ_{res} = -0.35%. With no strain present, the magnetic layer has energy maxima in the out-of-plane axis (z) while the minima and the saddle points are along the x and y axis respectively as shown in Figure 2.11(c, left). The presence of a small strain (less than the critical strain for PMA) manifests itself as a reduction of the out-of-plane energy barrier by introducing a small perpendicular anisotropy less than that of the shape anisotropy.

As the out-of-plane energy barrier becomes less than the in-plane energy barrier, the positions of the energy maxima and the saddle points gets interchanged (see Figure 2.11(c, right)). This results in a change of the magnetization relaxation dynamics from a highly precessional one to a fairly damped trajectory, being strongly dependent on the initial magnetization angles, or in other words, the phase of the arriving spin waves as highlighted earlier. For ϵ_{res} <-0.4%, the energy barrier between the stable in-plane magnetization states is markedly reduced resulting in loss of non-volatility. Beyond the critical strain of -0.48%, the magnet becomes PMA.

Note that there is butt-coupling of the [Co/Ni] multilayer waveguide and the CoFe layer of the ME cell. The voltage-driven strain-mediated magnetization switching of the transmitter ME cell from the in-plane to the out-of-plane configuration excites spin waves over a wide range of frequencies, as has been shown in [144]. However, only those frequencies which are above the cut-off frequency of the [Co/Ni] multilayer and CoFe layer are allowed to penetrate and propagate through the SWB and ME cell. The minimum cut-off frequency of the spin wave (corresponding to k = 0) calculated from the dispersion relation B.4 in both the materials are almost the same, around 11 GHz, giving rise to propagating spin waves with minimum reflection. The wide range of frequencies excited corresponds to a range of wave vectors following the dispersion relationship. A dominating wavelength of 210 nm has been extracted, similar to that reported in [145] that corresponds to a wave vector (k) of 3×10^7 m^{-1}. Figure 2.11(d) shows the spin wave transmission from the transmitter ME cell through the SWB to the detector ME cell and the frequency spectra along the length of the SWB, obtained from FFT of the x-component of the magnetization.

Figure 2.12(a) demonstrates the impact of ϵ_{res} on the switching success of the ME spin wave detector. The switching success has been defined as the probability of achieving an error-free logic functionality (buffer/inverter) in the presence of thermal noise. The narrow window of strain highlighted in the figure, within which the locations of the energy maxima and the saddle point interchanges, shows a dramatic increase in the switching success. It

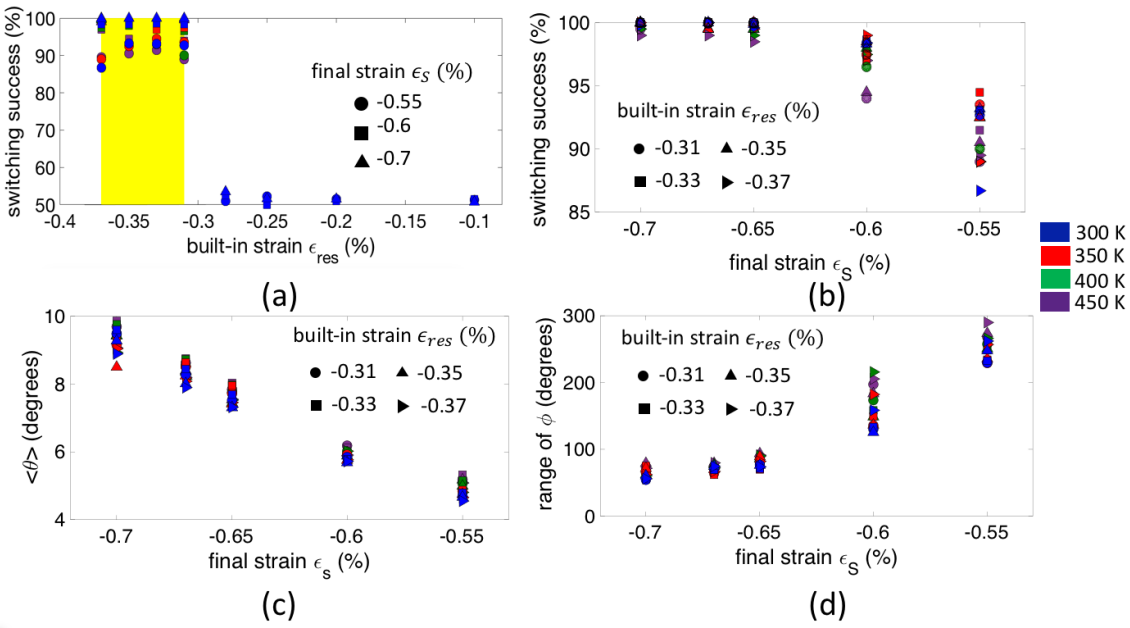

Figure 2.12: (a)Plot illustrating the dependence of the switching success on the built-in strain ϵ_{res},(b)Impact of the final strain ϵ_s on the switching success which stems from the effect on the detected mean amplitude (θ) and range of the phase (ϕ) of the spin wave as shown in (c) and (d), respectively. Symbols illustrate different final strains ϵ_s in (a) and built-in strains in (b-d) while colors indicate different temperatures (300 K-450 K).

is intriguing to find that there is yet another parameter that affects the switching success within this range of built-in strain: the magnitude of the final strain $\epsilon_s = \epsilon_{res} + d_{31}V/t_{PZ}$ due to applied voltage for in-plane to out-of-plane magnetization switching. As shown in Figure 2.12(b), the success rate increases with an increase in the magnitude of ϵ_s for all values of ϵ_{res}. The impact of ϵ_s stems from two distinct effects. Firstly, the mean amplitude of the spin waves ($< \theta >$) excited by the transmitter ME cell increases with the magnitude of ϵ_s as depicted in Figure 2.12(c). Secondly, the range of the detected phase of the spin wave (approximated as a 6σ deviation from the mean value) decreases with the increase in $|\epsilon_s|$ as shown in Figure 2.12(d). In other words, the capability to have a correct detection of the phase of the spin wave increases with the magnitude of ϵ_s due to - (i) generation of higher amplitude spin waves resulting in a higher signal to noise ratio (SNR) at the point of detection, and (ii) decrease in the inherent thermal fluctuations of the detector ME cell, i.e., a decrease in the thermal noise floor. To investigate the robustness of the proposed scheme

with respect to thermal noise, the effect of different temperatures has been included ranging from 300 K to 450 K in Figure 2.12. Overall, we see very little difference highlighting the robustness of the scheme relative to thermal noise.

2.6.3 Exchange-Spring System

Next, another interesting and a more flexible option to tailor the energy landscape and the spin configuration has been explored by placing the PMA SWB ($[Co(0.4)/Ni(0.8)]_{10}$) and the in-plane magnetized ($Co_{60}Fe_{40}$) layer one on top of the other as illustrated in Figure 2.13(a) and (b) [121]. Such a configuration, commonly referred to as exchange-spring [146, 147], exhibits a much stronger exchange-coupling between the ME cell and PMA SWB compared to the earlier structure, and by taking advantage of the strong competition between the shape anisotropy of the $Co_{60}Fe_{40}$ layer (favoring in-plane magnetization) and the PMA of the $[Co(0.4)/Ni(0.8)]_{10}$ multilayer, a desired magnetization tilt angle can be achieved. Additionally, the strong interlayer exchange coupling forbids the out-of-plane +z direction to have the energy maxima as shown in Figure 2.13(c), the condition which is desired to be achieved for thermal reliability. The impact of the change in the energy landscape has the same effect as explained earlier. The energy landscape and consequently the tilt angle can be varied by changing the thickness of $Co_{60}Fe_{40}$ layer (t_{ME}), and thus ensuring the non-volatility of the magnetization states under zero applied voltage.

The [Co/Ni] and the CoFe layers are coupled via volume exchange interaction as mentioned earlier. Similar to the case of built-in strain, voltage-driven strain-mediated magnetization switching of the transmitter ME cell excites spin waves with a wide range of frequencies. However, only those frequencies which are above the cut-off frequency of the [Co/Ni] multilayer and CoFe layer are allowed to penetrate and propagate through the SWB and ME cell. Figure 2.13(d) shows the spin wave transmission from the transmitter ME cell through the SWB to the detector ME cell and the frequency spectra along the length of the SWB showing the coupling of mode in [Co/Ni] to the CoFe layer.

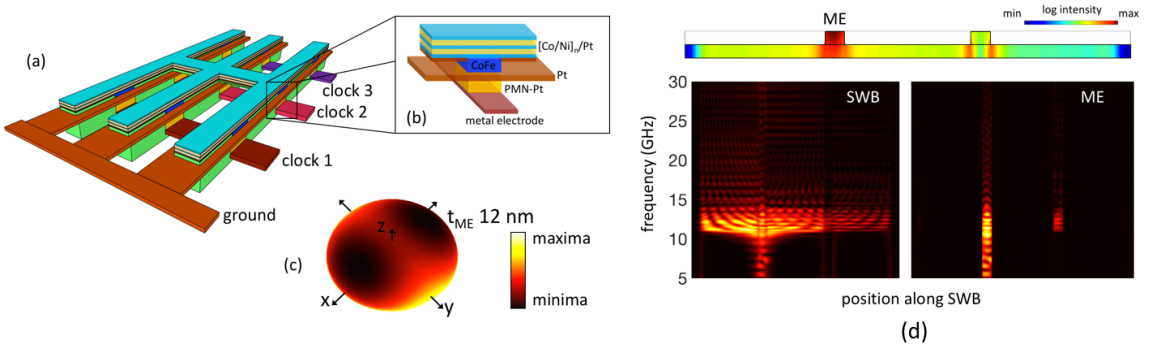

Figure 2.13: (a) Illustration of an alternative layout of a spin wave logic circuit, (b) Details of the main building blocks - ME cell and PMA SWB placed in a so-called exchange-spring configuration. (c) Energy landscape of the CoFe layer of the ME cell exchange coupled to the PMA Co/Ni SWB. (d) Spin wave transmission from the transmitter ME cell through the SWB to the detector ME cell and the frequency spectra along the length of the SWB, obtained from FFT of the x-component of the magnetization.

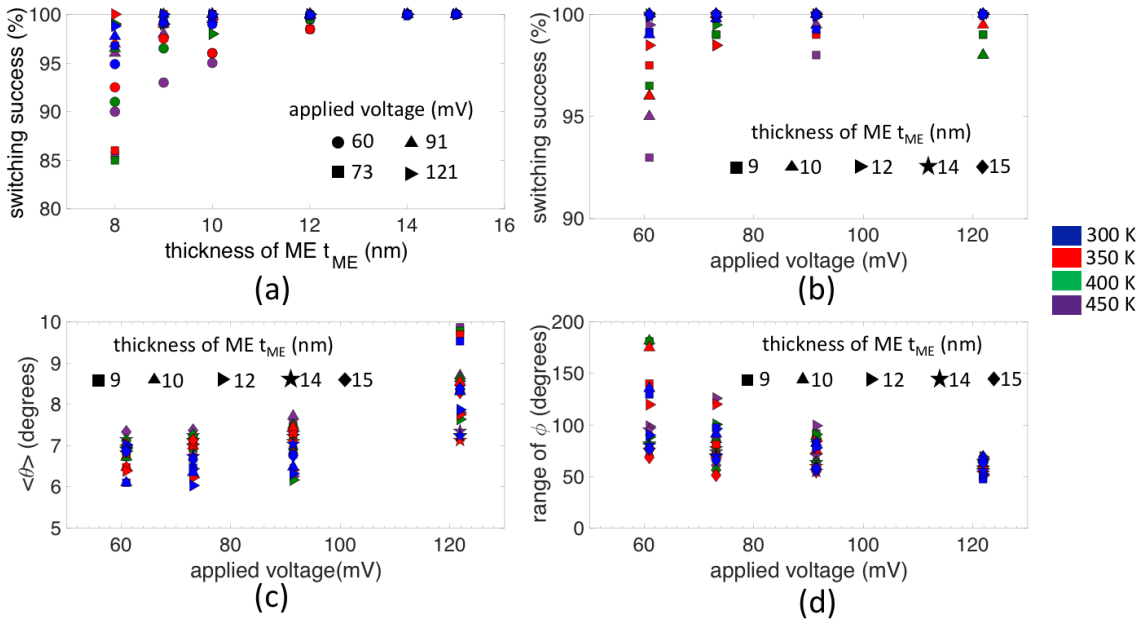

Figure 2.14: (a) Plot illustrating the dependence of the switching success on the thickness of the ME cell t_{ME}, (b) impact of the applied voltage on the switching success which stems from the effect on the detected mean amplitude (θ) and range of the phase (ϕ) of the spin wave as shown in (c) and (d), respectively. Symbols illustrate different applied voltages in (a) and thickness of the ME cell t_{ME} in (b-d) while colors indicate different temperatures (300 K-450 K).

Figure 2.14(a) demonstrates the impact of t_{ME} on the switching success of the ME spin wave detector. For relatively thin ME cell of around 8 nm, the reduction in the switching

success can be attributed to the low energy barrier (less than 40 k_BT) between the "zero-voltage" canted magnetization states. In contrast to the narrow window of required built-in strain, here, the switching success increases with t_{ME} and eventually saturates. This is because the condition for the energy maxima to be at +z direction is not enabled in all cases owing to the strong exchange coupling between the ME cell and the PMA SWB which prefers parallel spin alignment. It can also be seen that there is a dependence of the switching success on the applied voltage (Figure 2.14(b)) which can be explained by looking at the dependence of the detected mean amplitude ($< \theta >$) and the range of the detected phase (ϕ) of the spin wave on the applied voltage shown in Figures 2.14(c) and (d), respectively. We also investigate the robustness of our proposed scheme with respect to thermal noise by including the effect of different temperatures ranging from 300 K to 450 K in Figure 2.14.

2.6.4 Clocking Error

Establishing the fact that the proposed spin wave detection scheme is sensitive to the time of clocking, another error that enters into the picture and can have a significant impact on the reliability of the spin wave logic device is the clocking error. The clocking error can stem from sources such as clock jitter or transmitter-receiver clock skew. To study this error, the time of clocking normalized to the time period of the propagating spin waves has been varied and the probability of error-free logic functionality at each clocking time has been calculated. In addition to a change in the logic function of the device from an inverter to a buffer, one can also observe a switching margin in the range of T_{SW}/4 to T_{SW}/3 within which an error-free logic functionality can be ensured. In the simulations, for propagating spin waves with frequency around 11-13 GHz (T_{SW} = 77-90 ps), a switching margin of 20-30 ps has been observed. Assuming CMOS clocks operating in the frequency range of 3-5 GHz with 10% clocking error, one can expect to achieve such small clock margin although it may be challenging. Figure 2.15(a) and (b) show the simulation results obtained for the

two approaches mentioned earlier - built-in strain and exchange-spring, respectively.

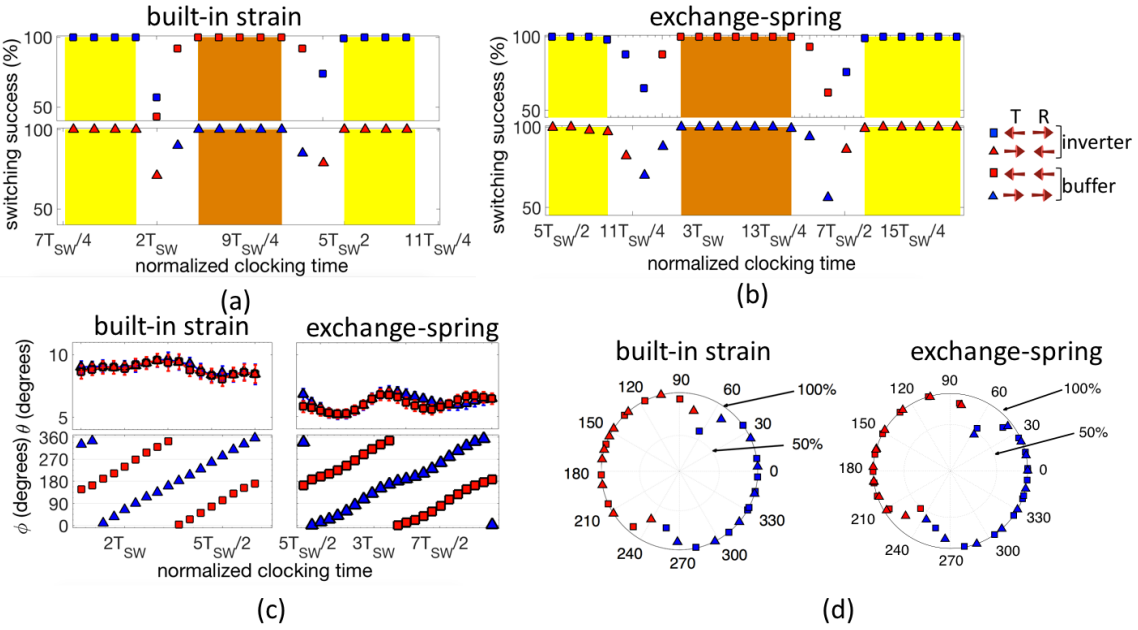

Figure 2.15: (a,b) Plot illustrating the impact of the time of clocking on the switching success for both the case of built-in strain and exchange-spring, respectively. In addition to a change in the logic function of the device from an inverter to a buffer, a switching margin in the range of $T_{SW}/4$ to $T_{SW/3}$ is observed within which an error-free logic functionality can be ensured. (c) Detected amplitude (θ) and phase (ϕ) of the spin wave as function of the time of clocking. Note the error bars indicate the deviation (σ_ϕ) from the mean value due to the presence of thermal noise. (d) Switching success as a function of the detected mean phase. An error-free logic functionality is achieved if the detected phase falls within the window from 280^o through 0^o to 20^o, i.e. 100^o, or from 100^o to 200^o.

To better understand the results, it is essential to look into the mean values of the detected amplitude ($< \theta >$) and phase ($< \phi >$) of the spin wave. A change in the time of clocking results in a change in the detected phase which dictates the direction of magnetization relaxation, in other words the functionality of the device (Figure 2.15(c)). Next, the switching success as a function of the detected mean phase ($< \phi >$) has been plotted as shown in Figure 2.15(d) for both the approaches. It is seen that if $< \phi >$ lies with the window from 280^o through 0 to 20^o, i.e. a 100^o margin, one ends up with an error free switching of magnetization to the +x direction while the window from 100^o to 200^o, also 100^o margin, results in an error free switching to -x. The reason for the tilt in the distri-

bution (asymmetric with respect to the line joining 90^o and 270^o) stems from the energy landscape and the constant energy trajectories [121]. It has to be emphasized that the results are in contrast to prior work that assumed the binary output (logic 1 or 0) would depend on the phase of the incoming spin wave falling in the range of 90^o to 90^o or 90^o to 270^o, respectively [148]. To have thermally reliable deterministic switching, the detected phase should fall within the window from 280^o through 0 to 20^o or from 100^o to 200^o.

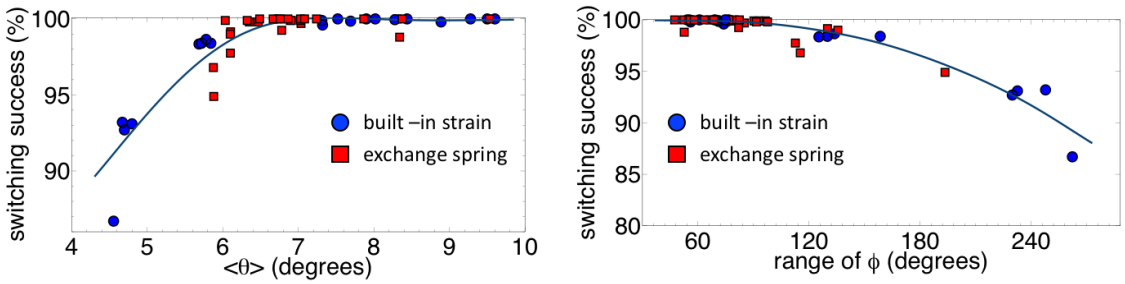

Figure 2.16: Dependence of the switching success on the detected amplitude (θ) and phase (ϕ) of the spin wave. A high switching success and error-free logic functionality can be ensured if the amplitude of the detected spin wave ($< \theta >$) remains higher than a threshold value of around 6^o and the detected phase falls within the window of 280^o through 0^o to 20^o or 100^o to 200^o with a maximum allowable ϕ range of around 100^o.

Based on what has been described until now, it is possible to set forth a design rule for ensuring the thermal reliability of the spin wave logic device [121]. As highlighted in Figure 2.16, combining results from both the approaches, a high switching success and error-free logic functionality can be ensured if the amplitude of the detected spin wave ($< \theta >$) remains higher than a threshold value of around 6^o and the detected phase falls within the window from 280^o through 0^o to 20^o or from 100^o to 200^o with a maximum allowable ϕ range of around 100^o. Note that the increase in the magnetic damping of the spin wave channel from the simulation value of 0.01 used here due to extrinsic contributions like sample in-homogeneity will result in a decrease of the mean amplitude of the spin wave ($< \theta >$) at the detector ME cell. The lowering of $< \theta >$ below the critical threshold for the case of enhanced magnetic damping ~ 0.1 will result in a decrease of the switching success of the ME spin wave detector. However, the thermal reliability and error-free logic

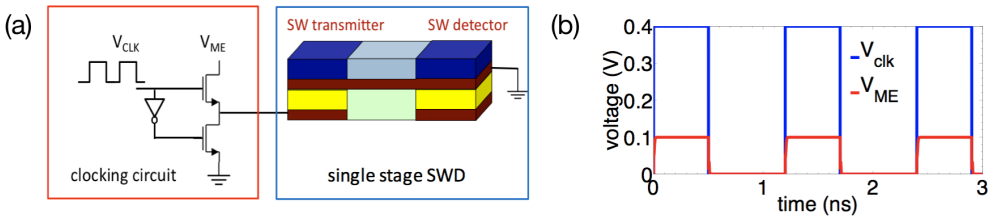

Figure 2.17: (a) Illustration of a single stage spin wave logic device along with the driving CMOS clocking circuit. (b) SPICE circuit simulation of the clocking circuit.

functionality can still be ensured by shortening the length of the spin wave channel which results in a higher spin wave amplitude ($< \theta >$) at the detector ME cell.

2.7 Performance Evaluation of Spin Wave Device

In this section, the energy-delay performance of the spin wave device, shown in Figure 2.17(a) along with the CMOS clocking circuit [65], has been estimated. The parameters used are highlighted in Tables 2.2, 2.1 and 2.3. The voltage induced strain-mediated out-of-plane anisotropy required for magnetization switching yields a low operating voltage V_{ME} of 0.1V and an intrinsic energy dissipation ($\frac{1}{2}\frac{\epsilon_0\epsilon_r A_{ME}}{t_{FE}}V_{ME}^2$) of 4.5 aJ keeping the switching delay to a minimum of 0.4 - 0.6 ns and a spin wave propagation time T_P of 0.2 ns. Following the clocking design delineated in Section 2.4, the single stage delay is estimated to be 2.4 ns. We perform HSPICE simulations for the clocking circuit shown in Figure 2.17(b) with the ME cell represented as a capacitance of $C_{ME} = \epsilon_0\epsilon_r A_{ME}/t_{pz}$ =0.9 fF and interconnect capacitance of $0.15 fF/\mu m$ and obtain an energy dissipation of 0.4 fJ. Note that the CMOS clocking circuit dissipates energy about $100\times$ larger than the intrinsic energy dissipation of ME cell. However, as will be highlighted in Section 3.6, each CMOS clock can drive approximately upto 250 ME cells following Elmore's delay calculation when we include interconnect resistance (20 $\Omega/\mu m$) and capacitance. Hence, the energy dissipation of the clocking circuit effectively comes down to 1.6 aJ per ME cell. See Table **??** for an overall comparison of performance.

CHAPTER 3

WAVE-BASED COMPUTING USING MAGNONS

3.1 Background and Prior Work

The spin wave device developed in Chapter 2 deviates from the traditional notion of behaving as just a gated-switch. In contrast, spin wave device itself posses the capability to perform arbitrary logic functions relying on wave interference and superposition. Shabadi et al. [59] and Khitun et. al. [79] suggested the idea of magnon-based spin-wave-logic functions (SPWF) and presented majority, weighted majority, and frequency-multiplexed majority devices. However, the proposals lacked rigorous micromagnetic modeling or simulation. Recently, it has been argued that performing non-conventional logic synthesis using "inverter" and "majority logic" as primitive gates may unravel the true potential of some of the emerging devices and harness their inherent advantages like majority voting capability. Klingler et. al. [149] simulated a spin wave based majority gate using in-plane magnetized spin wave bus. However, the demonstration suffered from the limitations of broken translational symmetry and anisotropic dispersion relation of backward volume spin waves that give rise to scattering processes where the waves interfere. A revised version was again put forward by Klingler et. al. [100], this time using out-of-plane magnetized film via external bias magnetic field. However, the device involved large dimensions (down to tens of microns) where excitation of higher order modes could not be avoided. The study of spin wave dynamics and interference at the nanoscale was still lacking.

So far, the key focus has been to design an efficient nonvolatile spin-wave logic device and interconnect, topology for spin-wave logic circuit, all-magnon-based circuits, namely, majority gate, spin-wave multiplexer, and magnon transistor. However, a key aspect of designing the spin-wave bus network, the crosstalk noise remains unexplored. A low crosstalk

noise level must be ensured for guaranteeing signal integrity. The crosstalk being a strong function of the spacing between the lines can become an issue as the lines get closer due to routing or near the points where the spin-wave buses merge in a logic circuit like a majority gate, and thus putting a limitation on the design, routing, and placement of spin-wave bus network. Additionally, any new emerging technology must be complimented by a fast and energy efficient transduction technology for signal conversion. But so far, any demonstration in this area remained missing.

3.1.1 Overview of Chapter

Shifting focus from designing just an efficient nonvolatile magnonic logic device, the aspect of crosstalk coupling noise between two co-planar spin wave bus has been investigated in Section 3.2. We investigated the crosstalk noise using rigorous numerical micromagnetics, and, using superposition of plus and minus modes described in Section 3.2.2), derived a compact physical model in Section 3.2.3. Building on the developed magnonic logic device along with crosstalk noise analysis, two primary logic gates - inverters and majority gates, that lie at the heart of wave-based computing, have been realized in Section 3.3. Finally, fast and energy-efficient spintronic transducers for signal conversion between the charge and spin domain have been discussed in Sections 3.4 and 3.5. Systematic analysis of the impact of the transducers on the performance of magnonic logic device in terms of energy and area overhead and overall performance evaluation of spin wave logic compared with 7 nm FinFET CMOS technology at the circuit level have been performed in Section 3.6. Finally, a SPICE circuit model for spin wave bus has been developed in Section 3.7 for seamless integration with other CMOS elements.

3.2 Crosstalk

A key aspect of magnonics-based computing, the crosstalk noise, remains unexplored. A low crosstalk noise level must be ensured for guaranteeing signal integrity. The crosstalk

being a strong function of the spacing between the spin wave bus can become an issue as they get closer due to routing or near the points where the spin wave buses merge in a logic circuit like a majority gate, thus putting a limitation on the design, routing and placement of spin wave bus network.

3.2.1 Crosstalk in a coupled spin wave bus interconnect system

For crosstalk in spin wave interconnects, two identical co-planar in-plane magnetized or the so called backward volume spin wave (BVSW) interconnects have been considered here with a uniform lateral edge-to-edge spacing (S) between them as shown in Fig. 3.1(a, left). The one line on the left is called the active line while the other line (right) is called the victim line. The active line is excited by a localized magnetic field sinusoidally varying in time. The excited spin wave signal in the active line propagates along the spin wave bus. Due to the dipolar coupling between the two nearby lines, a crosstalk noise is induced in the victim line [150]. Figure 3.1(a, right) shows the z-component of the magnetization in the two lines 4 ns after the time of excitation (steady state signal).

The steady-state amplitudes of the signals in the active ($S_A(x,t)$) and victim ($S_V(x,t)$) lines are analyzed first. The amplitude of the spin wave, defined as the peak value of oscillations in the z-component of the magnetization, is measured at various positions along the interconnect. For the active line, the externally applied magnetic field generates spin waves which propagate along the interconnect with decaying amplitude as shown in Figure 3.1(b). It is well established that the attenuation of the spin wave follows an exponential decay e^{-x/L_d} where L_d is the decay length. However this trend deviates for relatively small spacing (S = 10 nm) which can be accounted for the strong dipolar coupling between the two lines. The steady-state amplitude of $S_V(x,t)$ is shown in Figure 3.1(c). The crosstalk becomes prohibitively high as the spacing goes down below that of the width of the interconnect, thus putting a limitation on the layout schemes. The noise amplitude increases as a function of the distance from the point of excitation in the active line till it reaches

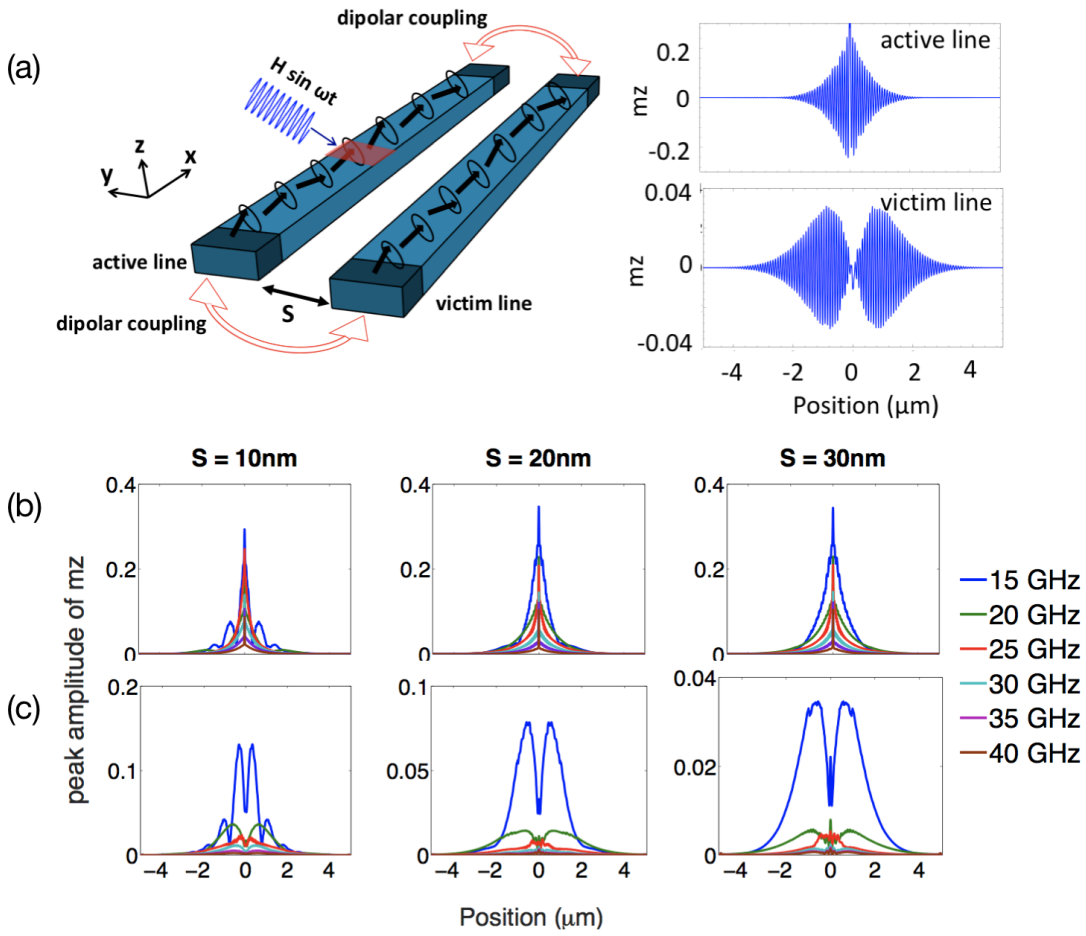

Figure 3.1: (a) Schematic for crosstalk analysis in BVSW interconnect. The active line is excited with a localized sinusoidal magnetic field. The excited spin wave signal propagates along the active line and induces a crosstalk noise in the nearby victim line. (b) Peak amplitude of (a) spin wave signal in the active line and (c) induced noise signal in the victim line as a function of the distance from the point of excitation in the active line marked as 0 μm for different frequencies of excitation. The subplots show the results for different edge-to-edge spacing between the lines.

a maximum, then shows an exponential decrease. The reason behind such a nature of the crosstalk noise will be explained in Section 3.2.2 using the superposition theorem. It must be noted that although crosstalk decreases for higher frequencies, the signal attenuation also increases. Hence, there is a trade-off between signal attenuation and signal integrity.

3.2.2 Crosstalk modeling using superposition

In RLC interconnects, a two-line coupled system can support two modes of signal propagation: plus and minus modes. The plus mode represents the solution to the coupled line configuration when both the lines are driven in-phase while the minus mode describes the situation when the lines are driven with 180° out-of-phase excitations. Using superposition theorem, the crosstalk noise in the victim line is calculated as a difference between the plus and minus modes [151].

Using an analogous approach [150], we consider two identical co-planar BVSW interconnects with a uniform lateral spacing (S) between them as shown in Figure 3.2(a). The plus or common mode represents the configuration when both the lines are excited by the same in-phase localized sinusoidal magnetic field (figure on the left). The minus or differential mode represents the case when both the lines are excited by the same magnitude but 180° out-of-phase magnetic field (figure on the right). The signal propagating in the active line and the induced noise in the victim line for the scenerio described in Fig. 3.1(a) can then be approximated as a superposition of these plus and minus modes. Note that for the plus mode, the propagating spin wave signals on both the lines are exactly in-phase at each point in time and along the length of the interconnects while for the minus mode, they are exactly 180° out-of-phase as shown in the insets (ii) and (iii) of Fig. 3.2(a). From henceforth, to avoid confusion, the plus and minus mode signals ($S_+(x,t)$ and $S_-(x,t)$ respectively) will be referred to as those propagating in the main line.

Next we formulate a way to model the plus and minus modes using only a single line instead of a rigorous full micromagnetic simulation of the two coupled lines by introducing a modified demagnetization tensor model. As mentioned earlier, in the plus mode, the propagating spin wave signals on both the lines are exactly in-phase at each point along the length of the interconnects while for the minus mode they are exactly 180° out-of-phase as shown in the insets (ii) and (iii) of Fig. 3.2(a). Hence, for the plus mode $\vec{m}_{self,j}$ = $\vec{m}_{ngbr,k}$ and we can add up the self and neighboring demagnetization tensors given by

(3.1). For the minus mode, only the x-components of $\vec{m}_{self,j}$ and $\vec{m}_{ngbr,k}$ are equal while the y- and z-components are of opposite signs. Hence, we can add the x-components of the demagnetization tensors but subtract the y- and z-components given by (3.2).

$$N^{+} = \begin{bmatrix} N_{xx}^{self} + N_{xx}^{ngbr} & N_{xy}^{self} + N_{xy}^{ngbr} & N_{xz}^{self} + N_{xz}^{ngbr} \\ N_{yx}^{self} + N_{yx}^{ngbr} & N_{yy}^{self} + N_{yy}^{ngbr} & N_{yz}^{self} + N_{xz}^{ngbr} \\ N_{zx}^{self} + N_{zx}^{ngbr} & N_{zy}^{self} + N_{zy}^{ngbr} & N_{zz}^{self} + N_{zz}^{ngbr} \end{bmatrix} \tag{3.1}$$

$$N^{-} = \begin{bmatrix} N_{xx}^{self} + N_{xx}^{ngbr} & N_{xy}^{self} - N_{xy}^{ngbr} & N_{xz}^{self} - N_{xz}^{ngbr} \\ N_{yx}^{self} + N_{yx}^{ngbr} & N_{yy}^{self} - N_{yy}^{ngbr} & N_{yz}^{self} - N_{xz}^{ngbr} \\ N_{zx}^{self} + N_{zx}^{ngbr} & N_{zy}^{self} - N_{zy}^{ngbr} & N_{zz}^{self} - N_{zz}^{ngbr} \end{bmatrix} \tag{3.2}$$

The plus and minus modes in a two-line coupled system can thus be modeled using a single line by solving the LLG equation (Equation 2.4) for one line using the modified demagnetization tensor model given by Equation 3.1-3.3.

$$\vec{H}_{demag,m}^{+} = -\sum_{n} N_{m-n}^{+} M_s \vec{m}_n^{+} \quad ; \quad \vec{H}_{demag,m}^{-} = -\sum_{n} N_{m-n}^{-} M_s \vec{m}_n^{-} \tag{3.3}$$

where N^{+} and m^{+} are the modified demagnetization tensor and magnetization distribution for the plus mode while N^{-} and m^{-} represent the minus mode. The active line signal $S_A(x,t)$ is then obtained as a summation of the plus and minus mode signals $\big[(S_{+}(x,t) + S_{-}(x,t))/2\big]$ while the victim line noise $S_V(x,t)$ is the difference between the two $\big[(S_{+}(x,t) - S_{-}(x,t))/2\big]$.

We compare the results obtained from the superposition technique with the full two-coupled-line system simulation results for the noise signal along the length of the victim

line 4 ns after the time of excitation. Figure 3.2(b) demonstrates good match between the two methods. Note that the spin wave signals in the two modes $S_+(x,t)$ and $S_-(x,t)$ differ from each other in terms of the attenuation and spatial wave vector. As a result, there exists a spatial phase difference between the two which varies along the length of the interconnect as shown in Figure 3.2(d). Near the point of excitation, $S_+(0,t)$ and $S_-(0,t)$ are almost in-phase thereby canceling out each other resulting in a low noise signal $S_V(0,t)$. The worst case scenario happens when $S_+(x,t)$ and $S_-(x,t)$ go out-of-phase (marked by black arrows in the figure) resulting in a low S_A and high S_V.

3.2.3 Compact analytical model for crosstalk

In Section 3.2.2, we have shown that the technique of superposition can be efficiently used to model and explain crosstalk in spin wave interconnects with reasonable accuracy. Here, we try to obtain an analytical expression for the crosstalk noise using this knowledge of superposition of the plus and minus modes. We approximate the spin wave propagating in the x-direction in the plus or minus modes as a sinusoidal wave in both space (x-direction) and time (t) with an exponentially decaying amplitude along the direction of propagation, given by the approximate analytical expressions

$$S_+(x,t) = A_+ e^{-x/\lambda_+} cos(k_+ x - \omega t - \phi_+) \quad (3.4)$$

$$S_-(x,t) = A_- e^{-x/\lambda_-} cos(k_- x - \omega t - \phi_-) \quad (3.5)$$

where A is the peak amplitude of the spin wave at the point of excitation, λ is the decay length, k is the wave vector related to the frequency ω through the dispersion relation, ϕ is the phase and $+$ and $-$ subscripts represent the plus and minus modes. We use the analytical expressions (Equations 3.4-3.5) to fit the propagating spin wave signals for the plus and minus modes obtained from micromagnetic simulations described in Section 3.2.2. The active line signal $S_A(x,t)$ is then obtained as a summation of the plus and minus mode

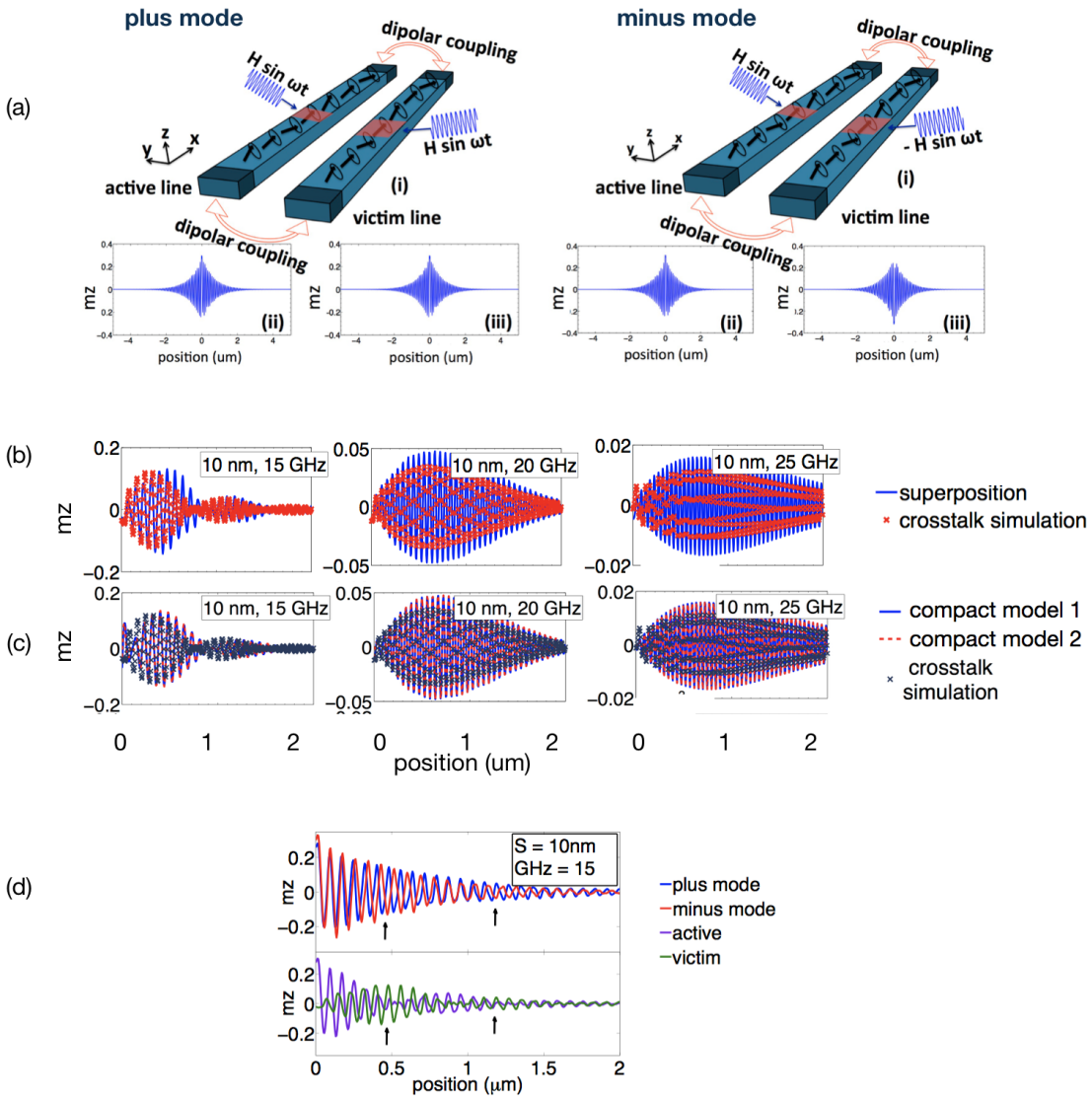

Figure 3.2: (a) Schematic for (left) plus mode and (right) minus mode analyses in BVSW interconnect. Both the lines are excited with a localized sinusoidal in-phase (or out-of-phase) magnetic field for plus mode (or minus mode). The spin-wave signals propagation along the length of the interconnect for each case is shown in (ii) and (iii). (b) Comparison between the result for crosstalk noise signal along the length of the victim line 4 ns after the time of excitation obtained from the superposition technique and the coupled-line crosstalk simulation. (c) Comparison between the compact model for crosstalk (eqn. 3.7 and 3.10) and the coupled-line crosstalk simulation results for the noise signal in the victim line 4 ns after the time of excitation. (d) Difference in the attenuation and spatial wave vector for the plus and minus modes giving rise to S_A and S_V and the reason for peak crosstalk longitudinal coupling strength.

signals $\left[(S_+(x,t) + S_-(x,t))/2\right]$ while the victim line noise $S_V(x,t)$ is the difference between the two $\left[(S_+(x,t) - S_-(x,t))/2\right]$ given by Equations 3.6 - 3.7.

$$S_A(x,t) = \frac{1}{2}(A_+e^{-x/\lambda_+}cos(k_+x - \omega t - \phi_+) + A_-e^{-x/\lambda_-}cos(k_-x - \omega t - \phi_-)) \quad (3.6)$$

$$S_V(x,t) = \frac{1}{2}(A_+e^{-x/\lambda_+}cos(k_+x - \omega t - \phi_+) - A_-e^{-x/\lambda_-}cos(k_-x - \omega t - \phi_-)) \quad (3.7)$$

Since the main factor governing the crosstalk noise is the difference between the spatial wave vectors k_+ and k_-, we can further simplify the above equations by defining an average amplitude and decay length

$$A_0 = \frac{A_+ + A_-}{2}; \lambda_0 = \frac{\lambda_+ + \lambda_-}{2} \quad (3.8)$$

Equations 3.6-3.7 then simplies to

$$S_A(x,t) = A_0e^{-x/\lambda_0}cos\left[k_1x - \omega t - \phi_1\right]cos\left[k_2x - \phi_2\right] \quad (3.9)$$

$$S_V(x,t) = -A_0e^{-x/\lambda_0}sin\left[k_1x - \omega t - \phi_1\right]sin\left[k_2x - \phi_2\right] \quad (3.10)$$

where k_1, k_2, ϕ_1 and ϕ_2 are defined as

$$k_1 = \frac{k_+ + k_-}{2}; \quad k_2 = \frac{k_+ - k_-}{2}; \quad \phi_1 = \frac{\phi_+ + \phi_-}{2}; \quad \phi_2 = \frac{\phi_+ - \phi_-}{2} \quad (3.11)$$

Figure 3.2(c) shows a good agreement between the compact physical model given by Equations 3.7 and 3.10) and the coupled-line crosstalk simulation results for the noise signal in the victim line 4 ns after the time of excitation.

3.3 Spin Wave Logic Gate

Using the proposed clocked non-volatile magnonic logic device developed in Chapter 2, we explore the two primitive logic gates required for wave-based computing: an inverter

(or buffer) and a majority logic gate.

3.3.1 Buffer/Inverter Logic Gate

The design of an inverter logic gate using spin waves have already been discussed in Chapter 2. For the sake of completion, a schematic of a single stage spin wave device acting as a buffer or inverter logic has been shown in Figure 3.3(a). It consists of an input and output ME cell connected via a spin wave bus. Figure 3.3(b) shows the magnetization dynamics of the input and output ME cells. At time t_1, a voltage is applied on the input ME cell and its magnetization starts to re-orient from +$\vec{x}$ towards +$\vec{z}$. This generates a spin wave with a specific phase which is detected from the second ME cell after time t_2, when its applied voltage is released. The output ME cell's magnetization stabilizes along +$\vec{x}$ (after time t_2), same as the initial magnetization of input ME cell; hence, acting as a buffer gate.

3.3.2 Majority Logic Gate

Unlike previous works on spin wave majority gates [100, 149], here a nanometer scale majority gate structure has been investigated [145]. In such a structure, the excitation of higher order modes can be avoided. Figure 3.3(c) shows a schematic of the majority gate. The structure consists of three merging perpendicular magnetic anisotropy (PMA) spin wave buses and four magneto-electric (ME) cells serving as three inputs and an output. For the initial study of the spin wave majority gates performance, we conducted single-arm excitation simulations and monitored the spin wave transmission in the complete structure. Figure 3.3(e), presents the spin wave amplitude (defined as $\sqrt{m_x^2 + m_y^2}$) averaged over time (i.e. 3 ns) in logarithmic scale. The amplitude transmission from input to output is $\sim 93\ \%$, defined as the ratio of the average intensity of the output to the average intensity of the input. This efficient transmission is due to the nanoscale dimensions of the structure in combination with the low damping values of the materials assumed. However, due to the symmetry of the structure there will be significant backflow as shown in Figure

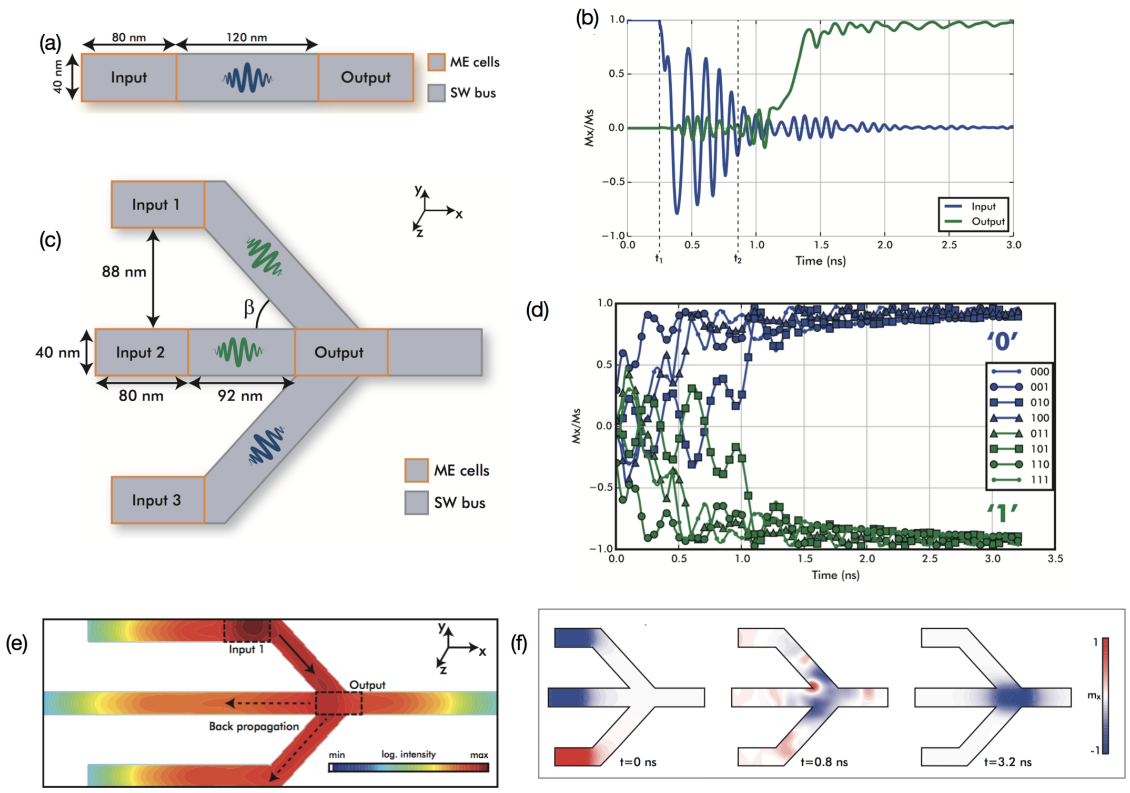

Figure 3.3: (a) Spin wave buffer structure with two ME cells, one acting as input (transmitter) and the other as output (detector), separated by 120 nm of spin wave bus. b) Magnetization dynamics of input and output ME cells. The output ME cell's magnetization stabilizes along $+\vec{x}$ same as the initial magnetization of input. (c) Geometry of the spin wave majority gate. Spin waves are excited by the three input ME cells (Inputs 1,2,3) and the majority result of the spin wave interference is detected by the output ME cell. The spacing between each arm is S = 88 nm. (d) Magnetization of the output ME cell for all possible input combinations resulting in the correct majority computation. (e) Spin wave amplitude transmission for single arm excitation, plotted in a logarithmic scale. Dashed arrows demonstrate the flow of back-propagated spin wave amplitude into the other input arms. (f) Spatial profile of x-component of magnetization of the majority gate with "110" input at different snapshots in time.

3.3(e). The back-propagations may increase the complexity of the spin wave dynamics and interference, but will not affect the states of the input ME cells due to the concept of non-reciprocity introduced in Section 2.4 via multi-phase clocking scheme. A key requirement is to ensure low crosstalk noise such that the dipolar coupling between the neighboring input arms would not impede the ME cells to completely switch out-of-plane and hinder the correct functionality. The analytical expression for the dipolar coupling in [152] and

the crosstalk modeling introduced in Section 3.2 is used to calculate the minimum spacing between the input arms. The minimum spacing of 56 nm has been verified by simulations. The fork-like structure we employ is geometrically symmetric. However, the side inputs (for input 1 and 3) are not *"magnetically symmetric"* since the spin wave propagation and dispersion depends on the shape anisotropy variation in the bend regions. A careful analysis allowed the spacing value S to be 88 nm where all three input signals have the most similar contributions to the output ME cell. A further optimization to make the three input arms equal in strength is to compensate for the extra path length introduced by the side arms due to bends or magnetically engineer the damping coefficient of the middle input arm[1].

Finally, the functionality of the spin wave majority gate is being investigated. Figure 3.3(f) illustrates an example operation of the spin wave majority gate, where the inputs are set to "110". After the three inputs are activated, the generated spin waves propagate towards the junction and interfere. At time t=0.8 nm, the detection is enabled which results in the output ME cell to stabilize at the correct majority result "1" (m_x = -1). Finally, to verify the complete logic behavior of the 3-input spin wave majority gate, we simulate all 2^3 possible input states and detect the result. The results of these simulations are summarized in Figure 3.3(d), where we observe that all inputs that have majority of "0" set the output ME cell magnetization along +$\vec{x}$ and all inputs that have majority of "1" set the output ME cell magnetization along -$\vec{x}$.

3.4 Spintronic Transducers for Interfacing with CMOS: Charge-to-Spin Conversion

The first stage of the spin wave logic circuit, called the charge-to-spin (CS) converter, involves translating information from charge to spin domain by switching the nano-magnet from a meta-stable to one of the low energy magnetization states. The switching can be determined via a voltage- or current-dependent external torque like transfer of angular momentum to the nano-magnet using spin-polarized current. We investigate two poten-

[1]The readers are referred to [145] for detail design about the majority gate

tial candidates - (a) spin-transfer torque (STT) switching and (b) spin-orbit-torque (SOT) switching using giant spin hall effect (GSHE) and/or Rashba-like interface effect.

3.4.1 Spin Transfer Torque Switching

Spin-transfer-torque (STT) arises due to a non-uniform flow of spin-angular momentum through a sample. For example, as shown in Figure 3.4(a), when a spin-polarized current (created by spin filtering through a magnetic layer) is filtered again by another magnetic layer whose magnetic moments are non-collinear with the first, the second magnet absorbs a portion of the spin angular momentum. The magnetization of the second magnetic layer exerts a torque on the flowing spins to re-orient them and the flowing electrons also exert an equal and opposite torque on the magnet. This torque is referred to as spin transfer torque (STT). The effect of STT is generally accounted for by an additional contributing torque term in the LLG Equation 2.4 [47]

$$\tau_{STT} = \eta(\theta)\frac{\mu_B I}{eVM_S}\vec{m} \times \left(\vec{m} \times \vec{m_{fixed}}\right) \tag{3.12}$$

where I is the current, V is volume of the magnet on which the spin-torque acts, $\eta(\theta)$ represents spin torque efficiency depending on the angle θ between the fixed and free magnet, and $\vec{m}$ and $\vec{m}_{fixed}$ are unit vectors of magnetization of the free and fixed layer, respectively. When a current is applied, the direction of the spin transfer torque predicted is either parallel or anti-parallel to the damping torque, depending on the sign of the current. For a sufficient current magnitude (above the critical current) that produced spin torque directed opposite to the damping torque, the magnetization can undergo full 180^o switching.

Figure 3.4(b) shows an STT based CS converter consisting of two MTJ stacks built on top of the ME cell with the fixed ferromagnetic layers pinned in the opposite directions ($\pm m_x$). The writing circuit consists of a CMOS inverter and 4 NFETs (N_1-N_4). First the magnetization of ME cell is switched from in-plane to out-of-plane by applying a voltage

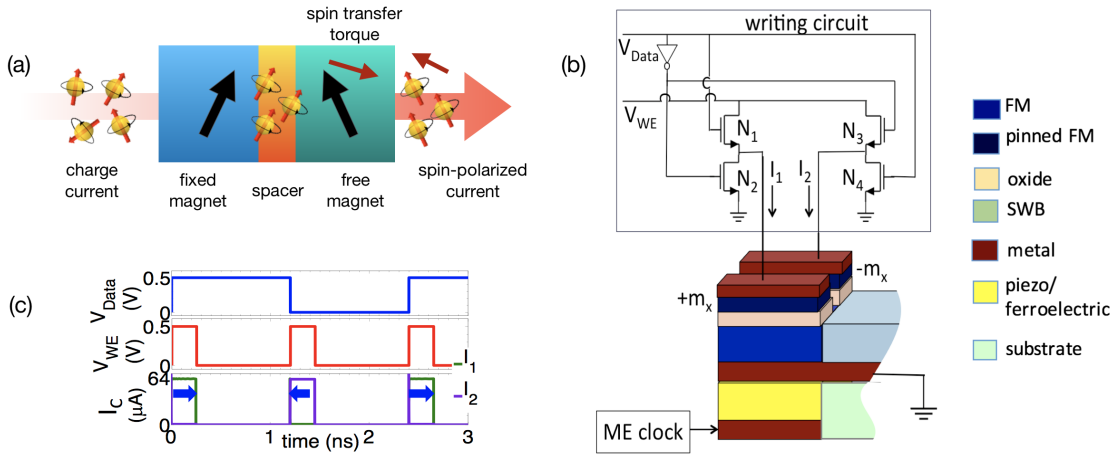

Figure 3.4: (a) Illustration of the spin transfer torque in a ferromagnet/nonmagnetic spacer/ferromagnet trilayer structure (b) Illustration of STT-based charge-to-spin converter using MTJ stacks on top of ME cell, along with peripheral CMOS cirucits. (c) SPICE simulation of the driver circuit.

V_{clk} across the piezoelectric layer. When V_{clk} of ME cell goes low, the write enable signal V_{WE} in the writing circuit is turned on. Depending on whether the data signal V_{Data} is high or low, either N_1 and N_4 or N_2 and N_3 are turned on, respectively. A high V_{Data} signal corresponding to bit "1" injects current I_1 through the left MTJ which gets spin polarized through the $+m_x$ pinned layer $I_s = I_1/\eta$ and switches the free FM layer from +z to +x direction. Similarly, a low V_{Data} signal writes bit "0" by switching the free FM layer to -x direction. Figure 3.4(c) shows the SPICE circuit simulation of the CMOS driver circuit.

3.4.2 Spin Orbit Torque Switching

Spin-orbit-torque have been recently unveiled as a new phenomena of generating spin torque in multilayer stacks consisting of oxide, ferromagnet (FM) and non-magnetic heavy metal (HM) with strong of spin-orbit coupling (SOC) without the requirement of a spin-polarizer ferromagnetic layer like in an MTJ. Two broadly accepted mechanisms have so far been proposed that exploit the coupling between electron spin and orbital motion and induce a non-equilibrium spin accumulation, which eventually generates a torque on the

magnetization.

The first is due to the bulk spin-Hall effect (SHE) which refers to the phenomena of conversion of un-polarized charge current (J_C) into transverse pure charge-less spin polarized current (J_S) as shown in figure 3.5(a). Experimental investigations ascribe the origin of the SHE to two distinct phenomena - spin-dependent extrinsic Mott scattering [48, 153] and spin-dependent deflection of electron's trajectory in the presence of spin-orbit (SO) coupled bandstructure giving rise to intrinsic SHE [154, 155]. The absorption of the spin current generated in the HM due to SHE creates a current-induced torque in FM capable of switching its magnetization. The efficiency of the conversion of the charge current in the HM to the spin current injected into the FM is quantified by the spin-Hall coefficient

$$\theta_{SHE} = \frac{2e}{\hbar}\frac{J_S}{J_C} \tag{3.13}$$

Assuming spin backflow which depends on the spin-mixing conductance $G^{\uparrow\downarrow}$ [156] to be the major contributor, the role of interfacial spin transparency [157, 158] is modeled as

$$T = \frac{2G^{\uparrow\downarrow}tanh(\frac{t}{2\lambda_s})}{2G^{\uparrow\downarrow}coth(\frac{t}{\lambda_s}) + \frac{\sigma}{\lambda_s}} \tag{3.14}$$

where t_{HM}, $\lambda_{s,HM}$ and σ_{HM} are the thickness, spin-diffusion length and conductivity of the HM, respectively. As the thickness of the HM becomes comparable to the spin-diffusion length, the spin-Hall current density inside the HM is reduced. This thickness-dependence is accounted for using drift-diffusion theory [81-83] as

$$J_s(t_{HM}) = J_s(\infty)\left[1 - sech\left(\frac{t_{HM}}{\lambda_{s,HM}}\right)\right] \tag{3.15}$$

to obtain the optimal HM thickness for maximum obtainable spin polarization ratio $P = I_S/I_C$.

The breaking of structural inversion symmetry at the interface gives rise to an additional

microscopic mechanism of SOT described by the Rashba model, similar to Figure 3.5(a). The electrons moving in an asymmetric crystal-field potential experience a net electric field $\vec{E}$, which gets transformed into a relativistic magnetic field that interacts with the electron's spin via spin-orbit interaction (SOI). The Rashba field is given as

$$H_R = \alpha_R(\vec{z} \times < \vec{k} >) \tag{3.16}$$

where α_R is the Rashba parameter defining the strength of SOI, $\vec{z}$ is parallel to$\vec{E}$ and $< \vec{k} >$ is the average electron wave-vector. The non-equilibrium spin density generated in this inversion-asymmetric system can then apply a SOT directly to the adjacent FM if the electron spins are exchange coupled to magnetic moment of the FM. The effective current-induced Rashba-field acting on the magnetization is expressed as

$$H_{eff,Rashba} = \frac{2\alpha_R m_e^*}{\hbar e M_S} P J_C(\vec{z} \times \hat{J}_C) \tag{3.17}$$

where m_e^* is the effective electron mass and P is the spin-polarization of the injected charge current $\vec{J}_C$. While the Rashba model treats the strong SOC at the interfaces but treats the transport in the HM (whose thickness is usually comparable to mean free paths and spin-diffusion lengths) as 2D, the SHE model treats the transport as 3D, but ignores any contributions from the modification of the spin-orbit coupling near the interface. Additionally, the proximity of HM with strong SOC to FM can also induce a moment in the HM and an enhanced SOC in the FM.

Both the SHE and Rashba effect can be modeled by two qualitatively equivalent additional torque terms in the LLG equation - the damping-like torque τ_{DL} and field-like torque τ_{FL}. The field-like torque arises from the component of the spin accumulation transverse to the injected current $\vec{J}$ in HM as

$$\tau_{FL} \approx \vec{m} \times \delta\vec{m}_\perp = \frac{\gamma\hbar J}{2eM_S t_{MF}} \epsilon_{FL} \vec{m} \times \left(\vec{m} \times \hat{J}\right) \tag{3.18}$$

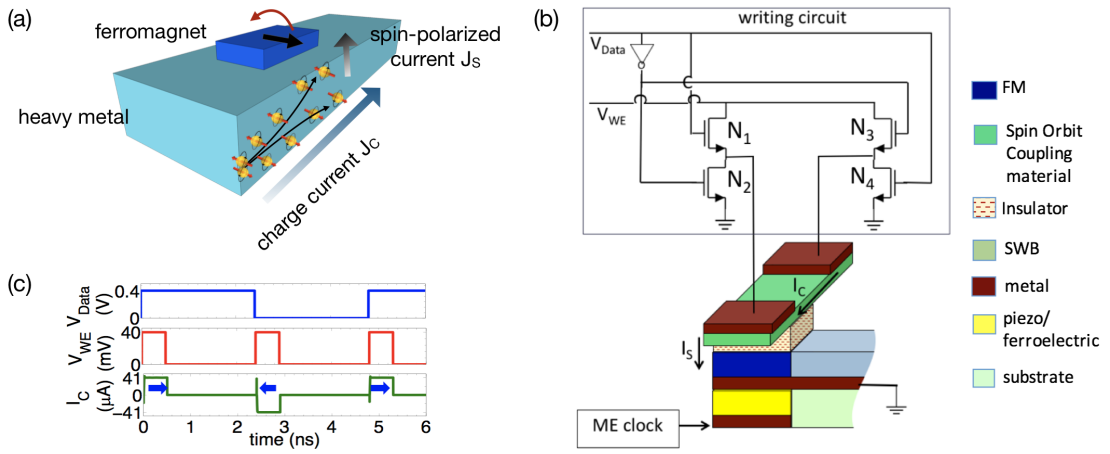

Figure 3.5: (a) Illustration of the spin orbit torque in a ferromagnet/heavy metal bilayer structure. (b) Illustration of SOT-based charge-to-spin converter using a heavy metal exhibiting high spin-orbit coupling on top of ME cell, along with peripheral CMOS cirucits. (c) SPICE simulation of the driver circuit.

where t_{FM} is the thickness of the FM. The damping-like torque can be equivalently calculated from the longitudinal component as

$$\tau_{DL} \approx \vec{m} \times \delta\vec{m}_{\parallel} = \frac{\gamma\hbar J}{2eM_S t_{MF}} \epsilon_{DL} \vec{m} \times \left(\vec{m} \times \hat{J} \right) \times \vec{m} \tag{3.19}$$

The efficiency of the field-like torque ϵ_{FL} and damping-like torque ϵ_{DL} can comprise of contributions from θ_{SHE}, T_{int} and α_R.

Figure 3.5(b) shows the proposed structure consisting of a SHE material exhibiting high spin-orbit coupling (SOC), like β-Ta, Pt, W and Bi_2Se_3 and high conductivity write electrodes, built on top of the ME cell. The writing circuit is the same as above with the current ensured to flow through the SHE material between the writing electrodes rather than through the FM layer to ground by properly adjusting the resistances in the current path or choosing an insulating FM layer. The chosen insulating FM layer also acts as a pure spin conductor, thus enhancing spin injection via the phenomena of *"spin-funneling"* [159]. During the time V_{WE} is high, depending on V_{Data}, I_c flows through the SHE material along (+/-) y-direction injecting (-/+) x-polarized spin current I_s along -z direction. Figure

Table 3.1: Material parameters of CS converter (SHE of Pt)

Parameter	Value	Units
Spin Hall angle θ_{SH}	0.1	nm
Conductivity σ	3.2x10^6	$\Omega^{-1}m^{-1}$
Spin mixing conductance $G^{\uparrow\downarrow}$	0.57x10^{15}	$\Omega^{-1}m^{-2}$
Spin diffusion length $\lambda_{s,HM}$	1.4	nm
Thickness t_{HM}	3.4	nm

3.5(c) shows the SPICE circuit simulation of the CMOS driver circuit. Here, we use SHE of Pt for CS transduction. The material parameters are listed in Table 3.1.

We obtain a delay of 1.3 ns from micromagnetic simulations. The energy dissipation from SPICE simulations for the writing circuit with Pt represented as a resistance of 45.58 Ω yeild 1 fJ/write which is 20$\times$ larger than the intrinsic energy dissipation of 50.6 aJ for the SHE obtained from micromagnetic simulation. We use a V_{WE} of 40 mV and a spin injection enhancement of 4-6 times using the phenomena of spin funneling that allows the write error-rate to be below 10^{-3} obtained from stochastic micromagnetic simulations. See Table **??** for an overall comparison of performance.

3.5 Spintronic Transducers for Interfacing with CMOS: Spin-to-Charge Conversion

Identifying an efficient transduction mechanism from the spin to charge variable is a crucial requirement for scaled beyond-CMOS spintronics logic devices. Here we discuss some of the feasible options for spin-to-charge (SC) converters - (a) using magnetic tunnel junction (MTJ) with high tunnel magnetoresistance (TMR), (b) magnetoelectric (ME) read-head and (c) inverse spin hall effect (ISHE) and interface Rashba-Edelstein effect (IREE).

3.5.1 Magnetic Tunnel Junction

Traditionally, read-out in a spintronic logic or memory (MRAM) utilizes the phenomena of tunneling magnetoresistance (TMR) [51, 160] in a magnetic tunnel junction (MTJ). During the read operation, depending on the relative orientation of the free and fixed layers, either

a low or high resistance state is read out by passing a sense current through the MTJ stack as shown in Figure 3.5(a). We consider an MTJ stack of [Ta/ NiFe/ MnIr/ CoFe/ Ru/ $Co_{40}Fe_{40}B_{20}$/ MgO (1.5 nm)/ CoFe/ Ta] that has been demonstrated to achieve a giant TMR of 277% with resistance-area product (RA_P) of 1060 $\Omega\mu m^2$ [161]. The MTJ stack built on top of the ME cell along with the CMOS read-out circuity is shown in Figure 3.5(b). The same clock V_{clk} used for clocking the ME cell is applied to the gate of the pMOS. The read-out operation is performed when V_{clk} is low and the magnetization is in one of the in-plane states ($+/-m_x$) storing either bit "1" or "0". As the sense current flows through the MTJ with a resistance either R_P (parallel configuration) or R_{AP} (antiparallel configuration) and a fixed resistance r from a matched MTJ, the nodal voltage V_N swings between a high and low value. The proposed scheme provides several advantages: (a) in contrast to an STT-RAM that uses the same MTJ for read/write, we use the MTJ for read-out only. Hence, we can have a thicker oxide that increases the TMR and the output voltage can directly drive a CMOS interfacing circuit without any bulky sense amplifier, (b) since we use a matched MTJ for series resistance, the circuit is reliable even if there is variation in oxide thickness.

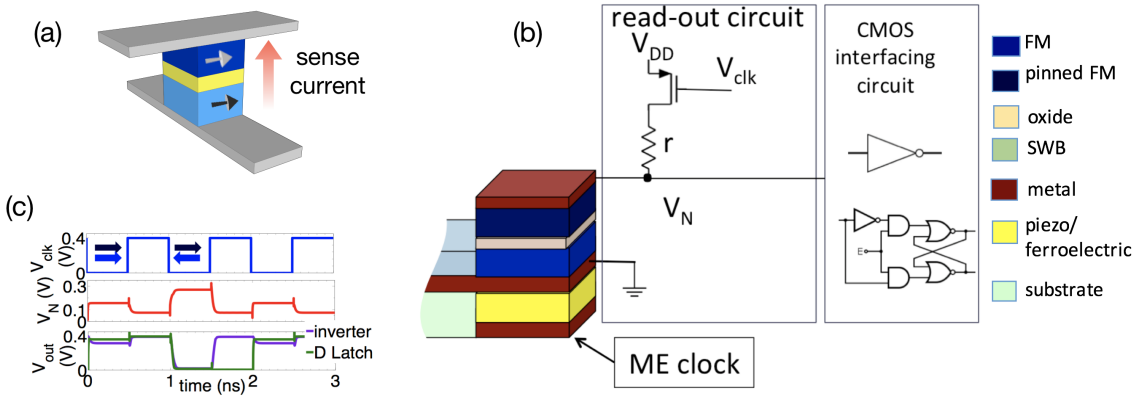

Figure 3.6: (a) Illustration of using TMR for read-out in a fixed magnet/insulator/free magnet structure trilayer. (b) Illustration of TMR-based spin-to-charge converter where MTJ stack is built on top of ME cell, along with peripheral CMOS cirucits. (c) SPICE simulation of the driver circuit.

Figure 3.5(c) shows the SPICE circuit simulations of the CMOS read-out circuit. The material parameters are listed in Table 3.2. The SPICE simulations of the SC converter

Table 3.2: Material parameters of SC converter (TMR of $Co_{40}Fe_{40}B_{20}$/MgO/CoFe)

Parameter	Value	Units
TMR	277%	-
Resistance-area product RA_P	1060 %	$\Omega\mu m^2$

yields an energy dissipation of 2.2-2.3 fJ considering inverter and D-Latch as the interfacing CMOS circuit, respectively, with an operating voltage of 0.4 V. This is nearly 10× higher than the intrinsic energy dissipation of 240 aJ in the read-out MTJ stack. See Table **??** for an overall comparison of performance.

3.5.2 Inverse Magnetoelectric Effect

An alternative to the previous scheme is to use the ME effect. Figure 3.7(a) shows a ME read-head [162] stack comprised of a ferroelectric layer sandwiched between two pinned ferromagnetic/antiferromagnetic layers that provide a dc exchange bias magnetic field. As the magnetization in the lower FM layer switches, the dipolar magnetic field H induces an output voltage $V = \alpha Ht$, where α is the magnetoelectric coefficient and t is the stack thickness. Although giant values of α = 50 V cm^{-1} Oe^{-1} have been reported with Pb($Zr_{1-x}Ti_xO_3$ (PZT) [163], the induced voltage is still within 0.1 V assuming a 100 Oe field, and would require a sense amplifier to interface with CMOS circuit. Using organic ferroelectrics like PVDF with reported α of 3700 V cm$^-1$ Oe$^-1$ [164] can help achieve an output voltage that can drive CMOS interface circuits without any additional bulky sense amplifier.

3.5.3 Inverse Spin Hall Effect and Rashba-Edelstein Effect

Recently, the phenomenon of spin-orbit effects such as the interface Rashba-Edelstein Effect (IREE) and the inverse Spin Hall Effect (ISHE)) have been proposed to convert spin currents into charge currents, preserving the information encoded in the spin polarization (utilizing resonant spin pumping and in the quasi-static non-local spin valve configuration)

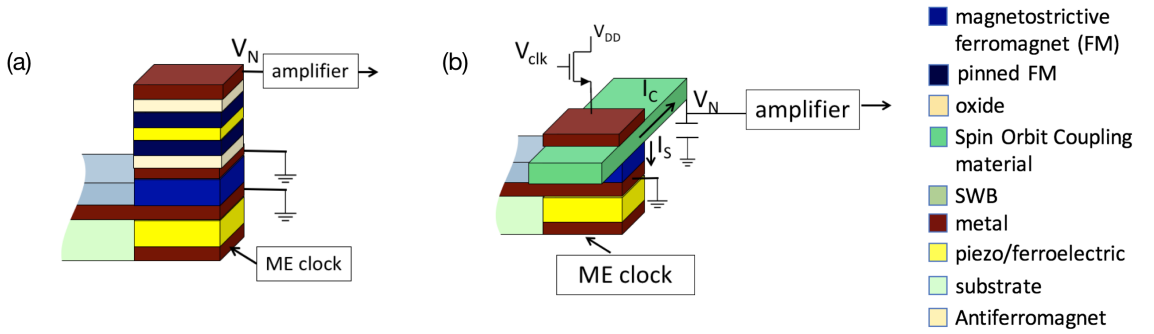

Figure 3.7: Illustration of (a) read-out scheme using inverse magnetoelectric effect and (b) inverse spin Hall/Rashba-Edelstein effect.

[52, 53, 165, 166]. A current through a nano-magnet can inject spin-polarized current into a stack of materials with a high spin-orbit coupling (like Bi/Ag, topological insulators, 2D materials, β-Ta, β-W, Pt)[2]. Consider the nano-magnets magnetization $\vec{m}$ pointing in the +$\vec{y}$ direction and spin current $\vec{J_S}$ is injected in the +$\vec{z}$ direction, a charge current $\vec{J_C}$ is generated in the +$\vec{x}$ direction. Alternatively, when the magnetization points in the -$\vec{y}$ direction, the charge current is produced in the -$\vec{x}$ direction. Hence, the magnetization orientation of the nano-magnet is transduced into the direction of the electric current.

Figure 3.7(b) shows the schematic of a feasible structure. The electrical current injected through the Cu/FM interface gives rise to a pure spin polarized current in the Cu channel due to spin accumulation at the interface. When a wire exhibiting high SOC is placed under the Cu wire, most of the spin current gets absorbed into the wire via bulk ISHE and/or IREE giving rise to a charge current

$$I_C = \frac{I_S}{w}\left[\theta_{SH}\lambda_s tanh\left(\frac{t}{2\lambda_s}\right) + \lambda_{IREE}\right] \tag{3.20}$$

where λ_{IREE} is the IREE length. Depending on the magnetization orientation, I_C either charges or discharges the capacitor. ISHE/IREE produces a spin to charge conversion efficiency of 0.1 with known materials and optimized widths, producing a net output voltage

[2]See [167] and the references therein for a comprehensive list of prospective materials

Table 3.3: Performance comparison

Component	Energy Dissipation	
	Intrinsic	CMOS peripheral
Intermediate ME cell	4.5 aJ	0.4 fJ *
Charge to spin converter	50.6 aJ	1 fJ
Spin to charge converter	240 aJ	2.2 fJ

* shared by 250 ME cells, 1.6 aJ/ME cell

V_N of around 0.1 V [167] and hence would require a sense amplifier to interface with CMOS circuit.

3.6 Overall Performance Evaluation

Table 3.3 shows the overall comparison of performance of the intrinsic components and peripheral CMOS circuits for the ME cell and spintornic transducers. As can be seen, the CMOS circuits disispate energy in fJ compared to the intrinsic energy dissipation of the components which is in aJ. This puts a huge overhead on the performance.

For estimating the energy overhead for the transducers, we consider a logic block of size N (number of ME cells) and a 3-phase clocking scheme as shown in Figure 3.8(a). From Elmore's delay calculation including interconnect resistance (20 $\Omega/\mu m$) and capacitance, we find that each clock can drive approximately upto 250 ME cells. The energy dissipation of the logic block excluding the transducers can be calculated by estimating the energy dissipation of each clock charging and discharging a total capacitance of the $250C_{ME}$. The overhead energy for $N_{i/p}$ inputs and $N_{o/p}$ output transducers can be calculated as $N_iE_{i/p} + N_oE_{o/p}$. Figure 3.8(b) shows the $\%$ overhead in energy considering total $N_{i/p} + N_{o/p}$ input-output transducers. It is seen that the $\%$ overhead goes down as the size of the logic block (number of ME cells) increases. However, even for a size of $2\text{x}10^4$ and 32 bit input/output (total 64), the energy overhead still remains at 25% and becomes even worse for 64 or 128 bits.

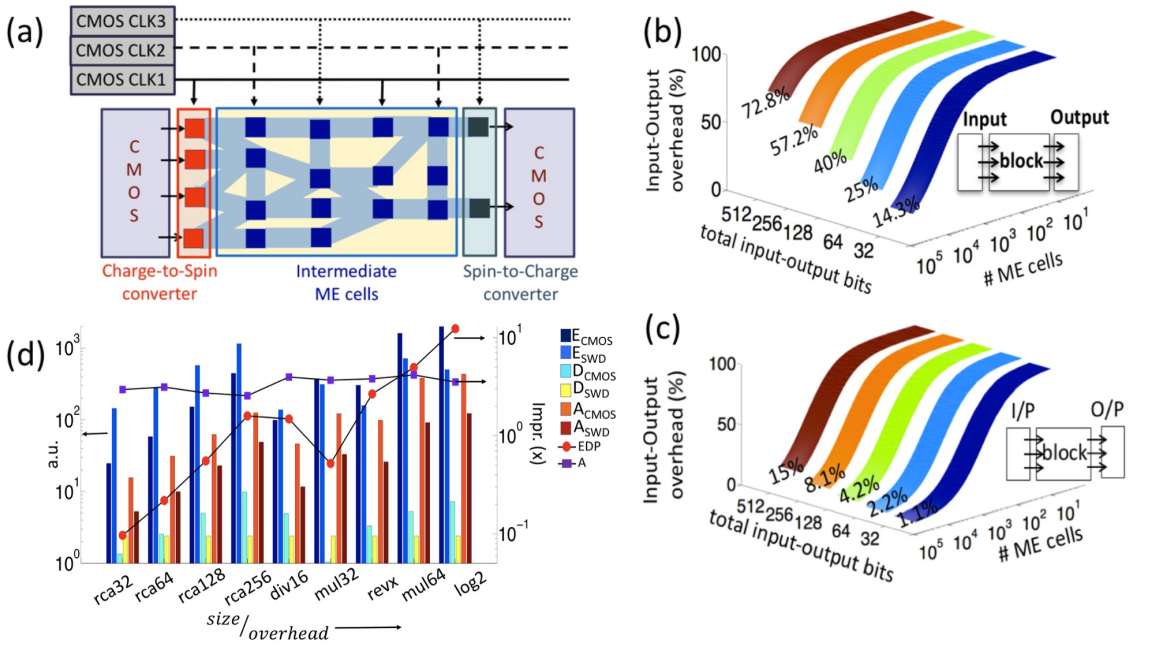

Figure 3.8: (a) Illustration of a SWD logic circuit architecture with CMOS peripheral circuitry, (b) Energy overhead imposed by transducers, (c) Area overhead imposed by transducers, (d) Comparison between SWD and 7nm CMOS in terms of area (A), energy (E) and delay (D).

For the delay estimation, if a program has a large number of instructions that need to be executed without any data dependencies, it can take the advantage of the pipeline structure of the SWD block by fetching input data at each clock cycle. The overall execution time per instruction is application dependent. At the optimal situation, the delay is equal to the clock cycle period of 2.4 ns, which is applicable to all types of instructions.

The area of a CMOS inverter is calculated following [40] as $160F^2$, where the minimum feature size F = 7nm. The area for nFETS is calculated assuming 50% area overhead with fin pitch of 3F, contact pitch of 4F and number of fins N_f. Figure 3.8(c) shows the % overhead in area considering $N_{i/p}$ input, $N_{o/p}$ output and $N_{i/p} + N_{o/p}$ input-output transducers. The area-overhead follows a similar trend as energy with less detrimental effect compared to energy.

Finally, we evaluate the performance of SWD in terms of the area, energy and delay and

compare it with the CMOS implementation at the circuit level as shown in Figure 3.8(d). A variety of circuits are synthesized using the Synopsys Design Compiler. The cell library is adopted from the 7nm FinFET technology. SWD-based circuits are evaluated based on MIG optimization [62]. On an average SWD shows a 3× improvement in terms of area compared to CMOS and upto 10× improvement in energy-delay product (EDP) for large complex circuits with low overhead. For smaller circuits like ripple carry adders (RCA), the energy overhead for transducers overshadows any gain achieved in terms of area.

3.7 SPICE Circuit Modeling

Due to the potential application of spintronic devices, simulation tools are required that can allow direct interfaces between magnetic and other CMOS and microelectronic circuit simulation tools, and thus avoid the electric and magnetic circuit simulations to be carried out separately. Here, we provide a physics-based SPICE compact circuit model for spin wave interconnect and use it to simulate the SWB structure [144]. The proposed SPICE spin wave model for micromagnetic simulation of spin waves is based on finite difference numerical micromagnetics. The three components of magnetization unit vector $\vec{m} = [m_{x,i}, m_{y,i}, m_{z,i}]$ in each domain are represented in the SPICE circuit as three node voltages $V(m_{x,i})$, $V(m_{y,i})$ and $V(m_{z,i})$. To simplify the model and since we are interested in having a narrow spin wave bus with widths in nanometers, we discretize the structure only in the x-direction which is along the wire. We compared OOMMF simulations with and without discretization along y and z-axes, and found a negligible difference.

3.7.1 Representing the LLG Equation using SPICE Model

The LLG equation given by Equation 2.4 can be modified as follows:

$$\frac{\mu_0(1+\alpha^2)}{\gamma}\frac{d\vec{m}}{dt} = -\mu_0(\vec{m} \times \vec{H}_{eff}) - \mu_0\alpha[\vec{m} \times (\vec{m} \times \vec{H}_{eff})] \tag{3.21}$$

We can further expand the cross products and write Equation 3.21 as a system of coupled equations,

$$\begin{aligned}
\frac{\mu_0(1+\alpha^2)}{\gamma}\frac{dm_x}{dt} &= \mathcal{F}(m_x, m_y, m_z, H_{eff,x}, H_{eff,y}, H_{eff,z}) \\
\frac{\mu_0(1+\alpha^2)}{\gamma}\frac{dm_y}{dt} &= \mathcal{G}(m_x, m_y, m_z, H_{eff,x}, H_{eff,y}, H_{eff,z}) \\
\frac{\mu_0(1+\alpha^2)}{\gamma}\frac{dm_z}{dt} &= \mathcal{H}(m_x, m_y, m_z, H_{eff,x}, H_{eff,y}, H_{eff,z})
\end{aligned} \tag{3.22}$$

Comparing Equation 3.22 with the relation

$$C\frac{dV(t)}{dt} = I(t) \tag{3.23}$$

for a simple capacitor circuit, we can model the quantity $\frac{\mu_0(1+\alpha^2)}{\gamma}$ as a capacitive element and the functions $\mathcal{F}, \mathcal{G}$ and $\mathcal{H}$ as three non-linear voltage dependent current sources. The schematic of the SPICE circuit model for LLG equation is shown in Figure 3.9(a). In our SPICE circuit, the m_x, m_y and m_z represent the three nodes whose voltages $V(m_x)$, $V(m_y)$ and $V(m_z)$ emulate the three components of magnetization unit vector $\vec{m}$. The voltage-dependent current sources $I_{m,x}$, $I_{m,y}$ and $I_{m,z}$ represent the functions $\mathcal{F}, \mathcal{G}$ and $\mathcal{H}$ of (3.22). The three voltage-dependent voltage sources $H_{eff,x}$, $H_{eff,y}$ and $H_{eff,z}$ represent the three components of the effective field $\vec{H}_{eff}$ given by (2.7).

3.7.2 Exchange Field Calculation

The discretized exchange field for the i^{th} domain is implemented in SPICE model by summing over three cells including only the nearest two neighbors along the x axis (neglecting any discretization along the width (y) and thickness (z)). Thus the simplified discretized exchange field term for each domain is modeled as a voltage dependent voltage source, depending on the node voltages corresponding to its own domain (i) and the two nearest

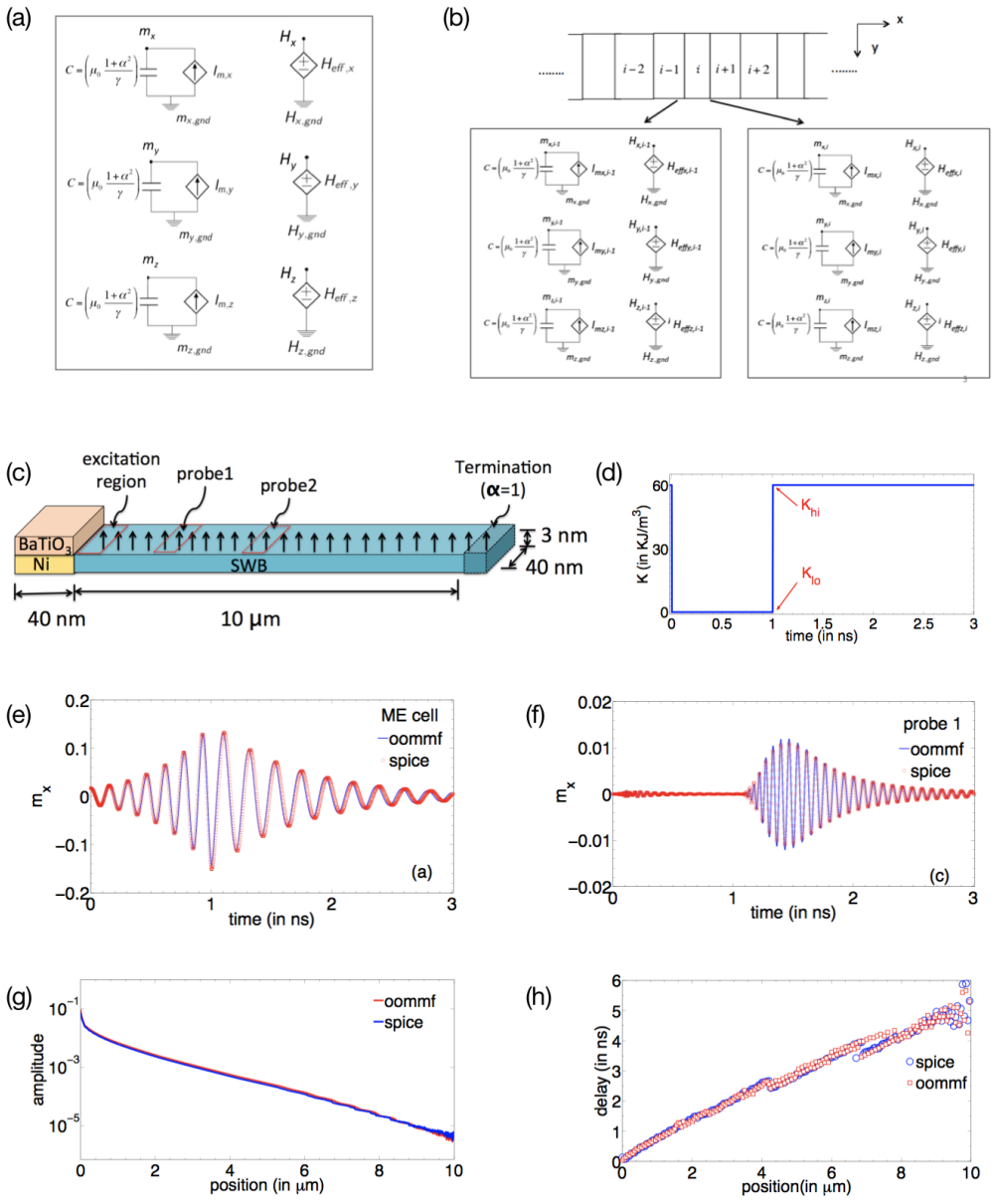

Figure 3.9: (a) Equivalent SPICE circuit model for the LLG equation. (b)Equivalent SPICE circuit for solving the LLG equation in each domain of the ME cell and SWB. Discretization of the ME cell and SWB is done only along the x-axis. (c) Illustration of a SWB with PMA excited by a ME cell (Ni/BTO). (d) Changes in the perpendicular anisotropy K from 60 to 0 kJ/m3. The voltage pulse is applied for 1ns. (e, f) x-component of the magnetization in the (ME cell and probe1 as a function of time. The pulsewidth for change in anisotropy is 1 ns. (g) Attenuation of the peak amplitude of the spin wave as a function of the position of the spin wave bus for 1 ns pulsewidth. (h) Delay of the spin waves as a function of positions of the SWB for 1 ns pulsewidth.

neighbor domains along the x axis $(i-1)$ and $(i+1)$.

$$V(H^i_{exch,p}) = \frac{2A}{\mu_0 M_s} \frac{V(m^{i-1}_p) - 2V(m^i_p) + V(m^{i+1}_p)}{|\Delta_x|^2} \tag{3.24}$$

where $p = x, y$ and z.

3.7.3 Anisotropy Field Calculation

Let the unit vector defining the uniaxial anisotropy axis be $\hat{u} = [c_x\hat{x}, c_y\hat{y}, c_z\hat{z}]$. The anisotropy field term for the i^{th} domain in a discretized form is implemented in SPICE as:

$$V(H^i_{aniso,p}) = \frac{2K}{\mu_0 M_s}\big[V(m^i_x)c_x + V(m^i_y)c_y + V(m^i_z)c_z\big]c_p \tag{3.25}$$

where $p = x, y$ and z.

3.7.4 Demagnetizing Field Calculation

We use the discretized demagnetization formulation to model the demagnetization field term in our SPICE model. This computation requires summation over all the domains in the sample. Traditionally, fast Fourier transform (FFT) is used to carry out the computation. To simplify our SPICE model, we make an assumption. We find that for a straight parallelepiped wire discretized only along the x axis, we have only three non-zero terms N_{xx}, N_{yy} and N_{zz} in the demagnetization tensor matrix N (2.9). We further see that since the value of these tensor elements depend solely on the distance between the domains, for any domain the value of the tensor elements decreases fast enough and can be neglected after the fifth neighboring domain. Hence, in our SPICE model, we assume a 5 nearest neighbor approximation. With this assumption, we can write the simplified demagnetizing field for our SPICE model as:

$$\begin{aligned} V(H_{demag,p,i}) \;=\; & -M_s[N_{p,i}V(m_{p,i}) + N_{p,i\pm1}V(m_{p,i\pm1}) + N_{p,i\pm2}V(m_{p,i\pm2}) \\ & + N_{p,i\pm3}V(m_{p,i\pm3}) + N_{p,i\pm4}V(m_{p,i\pm4}) + N_{p,i\pm5}V(m_{p,i\pm5})] \end{aligned} \tag{3.26}$$

where $p = x, y$ and z.

3.7.5 Boundary Condition Implementation

We include the Neumann boundary condition ($\frac{\partial \vec{m}}{\partial \hat{n}} = 0$) in our SPICE model which changes the expression for calculating the exchange field (Equation 3.24) at the edges. Since the boundary condition does not affect the second order terms (anisotropy, Zeeman and demagnetization) critically, their expressions remain unaltered at the edges. Thus the effective field in each domain can be computed as the summation of the exchange, anisotropy, demagnetizing and the applied fields:

$$V(\vec{H}_{eff,i}) = V(\vec{H}_{exch,i}) + V(\vec{H}_{aniso,i}) + V(\vec{H}_{demag,i}) + V(\vec{H}_{app,i}) \tag{3.27}$$

3.7.6 Micromagnetic Model: The Multi-Domain Structure

As described earlier, our SPICE model is based on the finite difference micromagnetics method, where the LLG equation governing the dynamics of magnetization is solved in each domain based on the effective field calculated in each domain. The schematic of such a multi-domain structure for the SPICE model is shown in Figure 3.9(b).

3.7.7 Validation of SPICE

For validating our SPICE model with micromagnetic simulations, we consider the proposed structure shown in Figure 3.9(c) consisting of a SWB having PMA excited by a ME cell. We consider a small perturbation in the magnetic configuration to excite spin waves (instead of 90^o switching of ME cell as earlier). Applying a small voltage pulse to the ME cell causes a reduction of the anisotropy K from $K_{hi} \approx 60KJ/m^3$ to $K_{lo} \approx 0$. The voltage pulse is assumed to be a step function applied from t = 0 to 1 ns as shown in Figure 3.9(d).

In Figures 3.9(e, f), we show the results of numerical simulations showing temporal evolution of the spin waves excited by the ME cell and propagating in the FM SWB. Mag-

netization for two representative regions - ME cell and probe 1 mentioned in Figure 3.9(c) are only shown. The amplitude of spin waves, defined as the peak value of oscillations in the x-component of the magnetization is measured at various positions along the SWB. For both OOMMF and SPICE, the peak amplitude is measured via post-processing of the output files in MATLAB. We see the amplitude of the spin wave packet decreasing as it propagates in the SWB. Figure 3.9(g) shows an exponential decay of the peak amplitude of the spin waves as a function of the distance from the source of excitation. As can be observed from Figure 3.9(e, f), there is a delay associated with the spin waves propagating in the SWB. We calculate the delay as the time taken by the peak amplitude of the spin waves to reach a given point in the SWB, shown in Figure 3.9(h). In this plot, there appears to be a degeneracy in the delay plot between the lengths of 7 and 8 μm. In reality, this is a rapid oscillation in delay versus length in this region. We speculate this oscillation to be a result of numerical errors incurred while post-processing. Overall, we see an excellent agreement of our proposed circuit model with the standard simulator in capturing the temporal variation of magnetization, the attenuation and delay of spin waves.

CHAPTER 4

WAVE-BASED COMPUTING USING PLASMONS

4.1 Background

4.1.1 Plasmonics - History

Lycurgus cup (see Figure 4.1) is a 4^{th} century Roman goblet currently located in the British Museum, London. What makes the cup noteworthy is that it appears to be of different color under different lighting condition: red when lit from behind and green when lit from in front. Perhaps accidentally, alchemists and glassmakers have taken advantage of what is today known as *"surface plasmon resonance"* when they incorporated tiny nanoparticles of gold and silver in colloidal form throughout the glass of the cup. In 1980s, researchers experimentally confirmed resonant behavior of mobile electrons on the surface of a metal when a light wave was directed at the interface between a metal and a dielectric. The oscillation of free electron density was termed *"plasmons"* and *"surface plasmons"* are those plasmons that remain confined to surface and interact strongly with light resulting in a *"surface plasmon polariton"*, aka. SPP wave. This was followed by the initiation of studying surface plasmons using Raman spectroscopy to determine the internal structure of a sample from scattered laser light. A further thrust came from Thomas Ebbesen who, in 1989, discovered the intensifying of the transmitted electromagnetic energy when a thin gold film containing millions of microscopic holes was illuminated. The term *"plasmonics"* was coined around 2000 by Dr. Harry Atwaters's group at Caltech to investigate this emerging field [168]. A new boost to this field came from the discovery of *"metamaterials"* in which the oscillations of electron can result in astonishing optical properties [169].

Figure 4.1: Lycurgus cup, a Roman goblet dating from the fourth century A.D., changes color because of the plasmonic excitation of metallic particles within the glass matrix.When a light source is placed inside the normally greenish goblet, it looks red.

4.1.2 Mathematical Description

The plasmon was initially described by David Pines and David Bohm in 1952 using the long-range electron-electron correlations [170]. Since plasmons are the quanta of classical plasma oscillations, they can be described using the well-known Maxwell's equations

$$\begin{aligned} \vec{\nabla} \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \quad ; \qquad \vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}, \\ \vec{\nabla} \cdot \vec{B} = 0 \quad ; \qquad \vec{\nabla} \cdot \vec{D} = \rho \end{aligned} \tag{4.1}$$

The simplest two-dimensional (2D) configuration sustaining a SPP wave is an interface of materials with permittivities (real part) of opposite sign. Most of the materials with negative permittivity (including popular noble metals, transparent conducting oxides, and doped semiconductors) can be fairly accurately modeled by a simple free-electron model, known as the Drude model, valid in frequency bands below the interband transition frequencies

$$\epsilon(\omega) = 1 - \frac{\omega_p^2}{\omega(\omega + i\Gamma)} \tag{4.2}$$

where ω_p and Γ are the plasma and collision frequency. Consider such a 2D geometry consisting of a dielectric ($\epsilon_d > 0$) material in the half-space z > 0 and a metal characterized with a complex, frequency-dependent permittivity $\epsilon_m(\omega)$ in the half-space z < 0. In such a system exhibiting invariance along the y-direction, i.e., wave propagation confined in the

x-z plane and wave vector along y k_y=0, SPPs are evanescent waves propagating along the x-axis characterized by wave vector k_x and exponentially decay along the z-axis, characterized by wave-vector $k_z = \sqrt{k_x^2 - k_0^2\epsilon}$, where $k_0 = \frac{\omega}{c}$. The propagating plane wave can have two types of polarization: transverse magnetic (TM) and transverse electric (TE) that are polarized in the propagation plane (p-polarized) and perpendicular to the propagation plane (s-polarized), respectively. The continuity of the components of the electromagnetic field across the interface along with the requirement of field confinement to the surface suggest that SPPs can only exist as TM polarized waves. The electric field component for such a TM polarized SPP wave can be written as

$$\vec{E}(z > 0) = (E_x^0, 0, E_z^d)e^{i(k_x x - \omega t)}e^{-k_{z,d}z} \tag{4.3}$$

$$\vec{E}(z < 0) = (E_x^0, 0, E_z^m)e^{i(k_x x - \omega t)}e^{k_{z,m}z} \tag{4.4}$$

where E_x^0 and $E_z^{d,m}$ are the amplitudes of the corresponding electric field components in the dielectric and metal, $k_z^{(d,m)} = \sqrt{k_x^2 - \epsilon_{d,m)}k_0^2}$ and

$$E_z^d = \frac{ik_x}{k_z^d}E_x^0; \quad E_z^m = -\frac{ik_x}{k_z^m}E_x^0 \tag{4.5}$$

The appropriate boundary condition for the normal electric field components results in the dispersion of the SPP wave at a single metal-insulator interface

$$k_x(\omega) = k_0\sqrt{\frac{\epsilon_m(\omega)\epsilon_d}{\epsilon_m(\omega) + \epsilon_d}} \tag{4.6}$$

The SPP modes considered in this chapter are confined in a multilayer system: a thin dielectric core layer (I) of thickness t sandwiched between two metallic claddings (II, III) resulting in a metal/insulator/metal (MIM) heterostructure. When two identical SPP modes start overlapping with each other for small layer thicknesses, the propagation constants of the symmetric and anti-symmetric (individual) mode combinations become different.

The only SPP mode surviving for all values t of the gap between metal surfaces, the so called gap SPP (G-SPP), is the mode exhibiting odd symmetry of the longitudinal electric field component E_x and, consequently, even symmetry of the transverse field component E_z. Using the appropriate boundary conditions for the normal and tangential electric field components as in the case of SPPs and the symmetry of the corresponding field component distributions, allows one to obtain the G-SPP dispersion relation

$$tanh\left(\frac{k_y^d w}{2}\right) = -\frac{\epsilon_d k_y^m}{\epsilon_m k_y^d} \tag{4.7}$$

For sufficiently small gap ($t \to 0$), one can use the approximation $tanh(x) \approx x$ resulting in the following approximate dispersion relation

$$k_x \approx k_0 \sqrt{\epsilon_d + 0.5\left(\frac{k_x^0}{k_o}\right)^2 + \sqrt{\left(\frac{k_x^0}{k_o}\right)^2 \left(\epsilon_d - \epsilon_m + 0.25\left(\frac{k_x^0}{k_o}\right)^2\right)^2}} \tag{4.8}$$

where $k_x^0 = -\frac{2\epsilon_d}{t\epsilon_m}$. For relatively large gaps, when the two SPP modes are only starting to interact, one can use the approximation $tanh(x) \approx 1 - 2e^{-2x}$ resulting in the following first-order corrected expression

$$\begin{aligned} k_x^{(1)} &\approx k_x \sqrt{1 - \frac{4\epsilon_d \epsilon_m}{\epsilon_m^2 - \epsilon_d^2} e^{-k_{z,d}^{(1)}}} \\ k_{z,d}^{(1)} = k_{z,d}^{(0)} \sqrt{1 + \frac{4\epsilon_m^2}{\epsilon_m^2 - \epsilon_d^2} e^{-k_{z,d}^{(0)}}}; &\qquad k_{z,d}^{(0)} = \sqrt{k_x^2 - \epsilon_d k_0^2} \end{aligned} \tag{4.9}$$

4.1.3 Modeling and Simulation

The dynamics of propagating SPP wave can be captured by solving the Maxwell's Equations 4.1 using the finite-difference-time-domain (FDTD) methodology. The equations are discretized in both space and time. Yee cells are used where the vector components of E- and H-fields are spatially staggered such that each E-field component is located midway

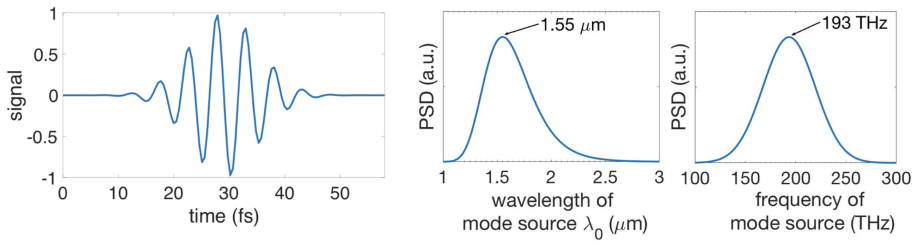

Figure 4.2: (a) Broadband Gaussian pulse signal injected by the standard mode source in Lumerical simulation. (b, c) Spectrum of the excitation signal with a center wavelength of 1550 nm and center frequency of 193 THz with a bandwidth of 43 THz.

between a pair of H-field components, and vice-versa. Further, a leap-frog algorithm is used in time where again the E- and H-field updates are staggered such that E-field updates are conducted midway during each time-step between successive H-field updates, and vice-versa.

For the rest of this chapter, full-wave 3-D simulations have been performed using the commercially available software Lumerical Solution [171]. Conformal mesh algorithm have been used with a specified mesh size of 5 nm for regular straight waveguides and a reduced mesh of 2 nm or 2.5 nm for bends. Absorbing boundary conditions based on perfectly matched layers (PML) are used to minimize reflections. SPPs were excited using the standard mode source in Lumerical Solutions to inject a fundamental guided mode into the plasmonic waveguide. The standard mode source injects a broadband Gaussian pulse signal as shown in Figure 4.2(a). Figures 4.2(b, c) shows the spectrum of the excitation signal with a center wavelength of 1550 nm and center frequency of 193 THz with a bandwidth of 43 THz. The phase of the source is specified as either 0^o or 180^o for simulating either a logic 1 or 0. Silver (Ag) is used as the metal in the simulations whose refractive index has been obtained from Palik's Handbook of Optical Constants [172]. The electromagnetic field and power monitor (2D x-normal) have been used in Lumerical to record the normalized transmission coefficients at the output. The time-domain electric field results are obtained using the time-domain monitor in Lumerical (2D x-normal for output E_Y and

2D z-normal for time-lapse results). The output electric field component E_Y has been calculated as a spatial average of the y-component of the electric field distribution, obtained from the time-domain monitor, over the cross-section of the output waveguide.

4.1.4 Plasmonics-Merging Photonics and Electronics at the Nanoscale

The scaling of CMOS technology has constantly resulted in faster transistors. However, efficient and fast movement of data across a microprocessor has faced major roadblocks as scaling of copper interconnect degrades the energy and delay. Optical interconnects such as fiber optic cables display three orders of magnitude capacity compared to electronic interconnect [55] and have been widely accepted as the means to transmit the vast amount of data across the globe. The rapid progress in CMOS compatible nano-photonics have resulted in revisiting the option of on-chip adaptability of optical interconnects for global wires [173]. Conjointly, photonic devices and circuits have been envisioned as a promising alternative to Si CMOS technology due to their high speed and low propagation loss [174]. However, the diffraction limit of light proves to be an obstacle for realizing nanoscale photonic devices as the dimensions approach the wavelength of light in the material. Surface plasmon polaritons (SPP) - electromagnetic waves propagating at the interface between a metal and a dielectric - can circumvent this problem by localizing the electromagnetic energy in dimensions much smaller than the diffraction limit [54, 55]. Recent advances in the field of plasmonics have witnessed the development of innovative wave-guiding schemes [175–181] and devices [182–189]. Various kinds of basic (AND, OR and NOT) and universal (NAND and NOR) plasmonic Boolean logic gates have also been proposed, relying on the intensity of the SPP wave as the computational variable and phase-dependent interference, capable of realizing the complete set of fundamental logic gates [187–189]. However, these CMOS based digital logic gate designs cannot exploit an important feature of plasmonic logic and wave computing, namely, the ability to execute majority voting efficiently. Deviating from the traditional path of CMOS oriented chip design, new logic

abstractions and synthesis techniques are being developed for the emerging nano-devices that are capable of reproducing the same CMOS logic circuitry with lower footprint and higher performance with only two building blocks inverter and majority logic gate [61].

4.1.5 Overview of Chapter

The focus of this chapter is to provide a comprehensive scheme for building nanoscale cascadable plasmonic logic. Contrary to the state-of-the-art plasmonic logic devices, the phase of the wave instead of the intensity has been used as the state or computational variable. This facilitates the utilization of the majority voting capability of the device inaccessible to amplitude-based wave computing. The basic building blocks have been introduced in Section 4.2. Slot waveguide (metal-insulator-metal MIM) configuration has been chosen due to its high field confinement capability (in nanometers) that aids the designing of nanoscale logic devices (Section 4.3). The critical aspect of crosstalk noise for designing dense on-chip integrated plasmonic logic has been discussed in Section 4.4. Building on top of this, the two primitive logic gates for enabling wave-based computing: inverter and majority logic has been designed in Section 4.5. The cascadability of these gates have been investigated up to three stages in Sections 4.6 and 4.8. This is sufficient to support interesting arithmetic primitives like adders and multipliers with limited bit-width. Larger arithmetic processor data-paths can then be composed from these primitives, however that lies outside the scope of this chapter. A unique referencing scheme at the output has also been proposed in Section 4.7 that can directly translate the information encoded in the amplitude and phase of the output SPP wave into the intensity of the output electric field or the output power, thus circumventing the challenging problem of tera-Hertz phase-detection of the SPP waves. Due to high throughput, the proposed scheme can be of use in highly parallel real-time signal processing applications that are arithmetic-heavy with strict timing requirements. A representative example of this, namely a pattern recognition system, has been briefly discussed towards the end of this chapter in Section 4.9.

4.2 Building Blocks

Based on the general model described earlier for any beyond-CMOS device, two basic building blocks can be again identified for plasmonic logic: (a) write and read unit for plasmonic excitation and detection, and (b) a channel that supports propagating plasmonic wave for transmission of information between the input and output.

4.2.1 Excitation and Detection of Surface Plasmon

On-chip propagating SPPs can be launched in several ways. Optical techniques involve matching the momentum of the incoming photon beam to that of the excited SPP wave by using Kretschmann or Otto configuration, or focusing an external laser radiation on grating couplers [190–192]. Compared to bulky optical excitation, electrical mechanisms can be directly integrated in the plasmonic circuit. Electrical excitation include using light-emitting diodes [193, 194], Si-based electrical source [195] and electron tunneling [196–198]. Phase coherency is an important requirement for our 3-input majority logic operation. Currently, phase coherent waves are not yet demonstrated for two independent emitters. However, provided sufficient input power, by splitting the output of a single emitter into three components and injecting them into the input waveguides, phase coherency can be assured. Since we rely on the phase of the SPP wave as the state or computational variable, the information can be written into the phase of the plasmonic wave by incorporating phase modulators such as Mach-Zehnder interferometers (MZI) [199] or shift-keying based resonators [200].

Compact detection of SPP is required either for signal conversion or data read-out. Several plasmon based photodetection techniques have been proposed like hot electrons generation that can tunnel across a Schottky-barrier producing photocurrent [201], using Ge nanoparticle for enhanced near-field absorption of light to produce photocurrent [202], using a metal-semiconductor-metal (MSM) photodetector [203], all-electrical detection based

on near-field coupling between guided plasmons and a nanowire field-effect transistor [204] and electrical detection of plasmons in metal-insulator-metal waveguide exploiting photodetection [205].

However, the emphasis of this work has been on building a nanoscale cascadable plasmonic logic; hence, we do not refer to any particular technique of excitation and detection which remains outside the scope of current research.

4.2.2 Plasmonic Waveguide

The past years have seen an active research in the field of plasmonic waveguide for on-chip communication [206, 207]. Surface plasmons can be confined in a simple three-layer structure with (a) an insulating layer sandwiched between two metal layers, aka, metal-insulator-metal (MIM) waveguide and (b) a metal layer sandwiched between two dielectric layers known as insulator-metal-insulator (IMI) waveguide. IMI waveguides are comparable to cylindrical nanowires that have been studied in the past for confining light to extraordinarily small lateral fields. However, the MIM waveguide has gained most attention due to its high field confinement capability (in nanometers) that may aid the designing of nanoscale logic devices [181, 189, 208]. It comes at a cost of higher loss and lower propagation length compared to IMI. Other waveguide candidates include channel plasmon and gap-plasmon. Recently, a hybrid plasmonic waveguide has been proposed by depositing a narrow dielectric ridge on a metal surface. The so-called dielectric load SPP waveguide exhibits good balance between optical confinement and propagation length [209, 210].

A comparative work by Zia et. al. [208] has established that only MIM waveguide can achieve deep subwavelength confinement with almost 4 orders of magnitude higher confinement compared to IMI. This allows tighter pitch for MIM waveguides enabling high-bandwidth dense on-chip integrated logic circuit. Hence, in this work, we choose a slot (metal-insulator-metal MIM) waveguide configuration due to its high field confinement capability (in nanometers) that aids the designing of nanoscale logic devices. Figure 4.3(a)

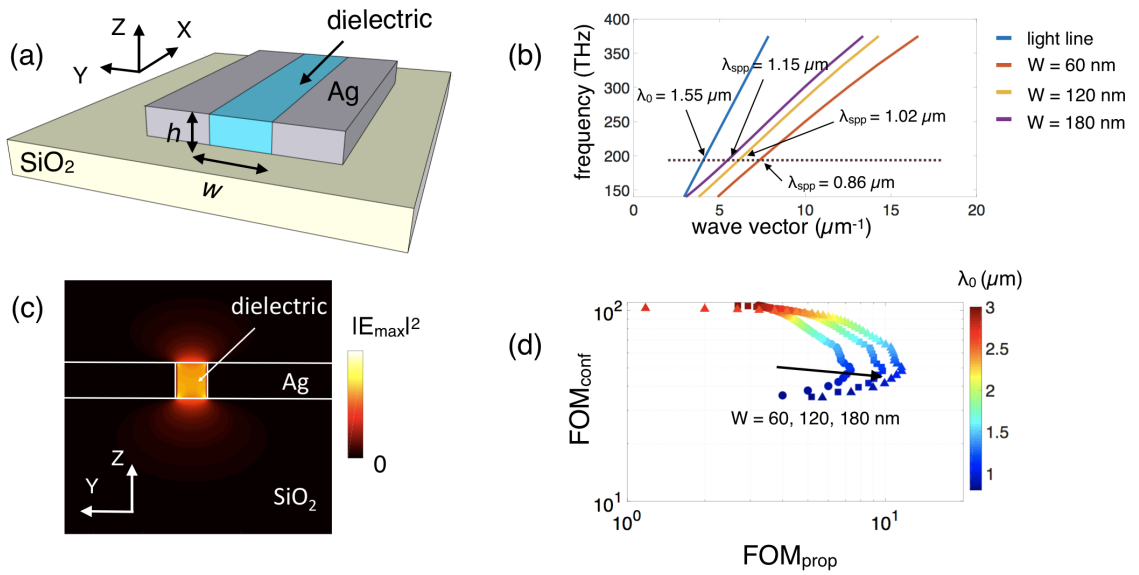

Figure 4.3: (a) Schematic of the metal-slot MIM plasmonic waveguide consisting of Ag on top of SiO_2 substrate and a dielectric of 1.5 refractive index, acting as a channel for transmission of information. (b) Calculated dispersion relation of the slot waveguide for gap widths of 60, 120 and 180 nm. (c) Fundamental plasmonic mode in a 60 nm wide metal-slot waveguide at λ_0 = 1.55 μm. (d) Two dimensional figure of merit (FOM) graph as a function of the wavelength λ_0 illustrating for our exploration space a good trade-off between the propagation and confinement at the chosen excitation wavelength of λ_0 = 1.55 μm.

shows the schematic of the slot plasmonic waveguide. Silver (Ag) on top of a silicon dioxide (SiO_2) substrate is used for the metallic structure while the dielectric is assumed to have a refractive index of 1.5. The refractive index of the surrounding air is set to 1. Simulation parameters are listed in Table 4.1.

4.3 Characterizing Plasmonic Waveguide

SPPs are electromagnetic waves traveling at the interface between a metal and a dielectric. In an MIM geometry, the two identical SPP modes overlap with each other for small dielectric (insulator) layer width, resulting in a so-called gap SPP (G-SPP). The G-SPP mode displays an odd symmetry of the longitudinal electric field component E_x and even symmetry of the transverse field component E_y. The electromagnetic fields are predominantly

Table 4.1: Simulation parameters for plasmonic waveguide

Parameter	Value	Units
Height (h)	100	nm
Width (w)	60-180	nm *
Excitation frequency (λ_0)	1.55	μm

* width increased at each stage to enhance transmission as explained later.

confined within the slot with the evanescent decay $e^{-k_y y}$ inside the metal described by the transverse wave vector k_y along the y-direction. Along the direction of propagation, the electromagnetic fields vary harmonically as $e^{i(k_x x-\omega t)}$ defined by the complex longitudinal wave vector k_x along the x-direction. The longitudinal wave vector k_x can be defined in terms of the permittivities of the metal ϵ_m and dielectric ϵ_d and free-space wavelength of light λ_0. The real part of the SPP wave vector can be further used to define the effective index of the plasmonic mode inside the waveguide as $n_{SPP}^{eff} = \frac{\lambda}{2\pi}\text{Real}(k_x)$. Using appropriate boundary conditions for the normal and tangential electric field components and the aforementioned symmetry of the corresponding field component distributions, the G-SPP dispersion relation can be obtained as [211, 212]

$$tanh\big(\frac{k_y^d w}{2}\big) = -\frac{\epsilon_d k_y^m}{\epsilon_m k_y^d} \tag{4.10}$$

with $k_y^{(d,m)} = \sqrt{k_x^2 - \epsilon_(d,m)k_0^2}$ and $k_0 = 2\pi/\lambda_0$. Approximate analytical expressions for the G-SPP dispersion relation for sufficiently small or relatively large gap width have been obtained in [183, 211]. Figure 4.3(b) shows the numerically calculated dispersion relation of the slot waveguide for three different widths (60, 120 and 180 nm). Since the emphasis of this work is on building a nanoscale cascadable plasmonic majority logic, we do not refer to a particular technique of excitation and use the standard mode source in our Lumerical simulations to inject a fundamental guided mode into the plasmonic waveguide. We choose an operating wavelength of λ_0=1.55 μm (corresponding to a frequency of 193 THz) for the

mode source in Lumerical simulations. The corresponding wavelength dependent complex relative permittivity of Ag is -116.67+i11.65 while the relative permittivity of SiO_2 used here is 2.08. Note that the wavelength of the propagating SPP mode λ_{SPP} is different from λ_0 depending on the width of the waveguide as indicated by the dispersion relation in Figure 4.3(b). Figure 4.3(c) shows the fundamental plasmonic mode (electric field) distribution inside a 60 nm wide metal-slot waveguide at λ_0 = 1.55 μm suggesting deep subwavelength confinement. The maximum electric field intensity is located at the metal-dielectric interface around the two lower vertexes, consistent with the results of Pan et. al. [189].

The development of plasmonic logic is hindered by the dissipative loss. Because of optical to heat energy conversion [213], surface plasmons propagating along the interface of metal and dielectric decay. The propagation length usually depends on the material properties of medium, its geometry, frequency of operation, and field symmetries of the plasmon mode. To quantify the trade-off between the degree of confinement and the propagation loss and the degree of confinement, we calculate both the propagation length

$$L_p = \frac{1}{2Im[k_x]} \tag{4.11}$$

defined as the distance over which the propagating power decays up to $1/e$, and the evanescent decay length inside the metal

$$\delta = \frac{1}{Im[k_y]} \tag{4.12}$$

defined as the distance over which the field decays up to $1/e$ in the transverse direction [214]. The corresponding figures of merit for propagation and confinement are given by

$$FOM_{prop} = \frac{L_p}{\lambda_{spp}}; FOM_{conf} = \frac{\lambda_0}{\delta} \tag{4.13}$$

respectively. Note that there are various other definitions of plasmonic mode confinement involving the spatial extent of the energy [208, 215]. However, all of them are largely determined by the same exponentially decaying field outside the waveguide, so we believe that our definition of δ is sufficiently representative. Figure 4.3(d) shows the two dimensional figure of merit (FOM) graph [216] for our exploration space as a function of the excitation (free-space) wavelength λ_0 of the mode source in Lumerical simulations for the three different widths of the waveguide. The chosen wavelength of λ_0 = 1.55 μm illustrates a good trade-off between the propagation and the confinement.

4.4 Crosstalk

A critical aspect of designing dense on-chip integrated plasmonic logic is to ensure low crosstalk noise which puts a limitation on the routing and placement of the plasmonic waveguides. Choosing a MIM geometry add to our advantage since, compared to insulator-metal-insulator (IMI) waveguides, it enables higher confinement resulting in a tighter pitch (center-to-center distance between the adjacent waveguides) while maintaining a low crosstalk noise. In plasmonics, the crosstalk noise is defined as the coupling or overlap of modes between the adjacent waveguides resulting in a transfer of power from one waveguide to another. Consider two identical co-planar plasmonic waveguides as shown in Figure 4.4(a). The active waveguide is excited with an input power P_A. Due to coupling between the two waveguide, the power in the victim waveguide, also referred to as the "noise" signal, is given by

$$P_V(L) = P_A sin^2\left(\frac{\pi L \Delta n}{\lambda_0}\right) \tag{4.14}$$

where L is the length of the coupling region and Δn is the index difference between the two coupled modes. The coupling length L_c for any amount of power coupling to the victim

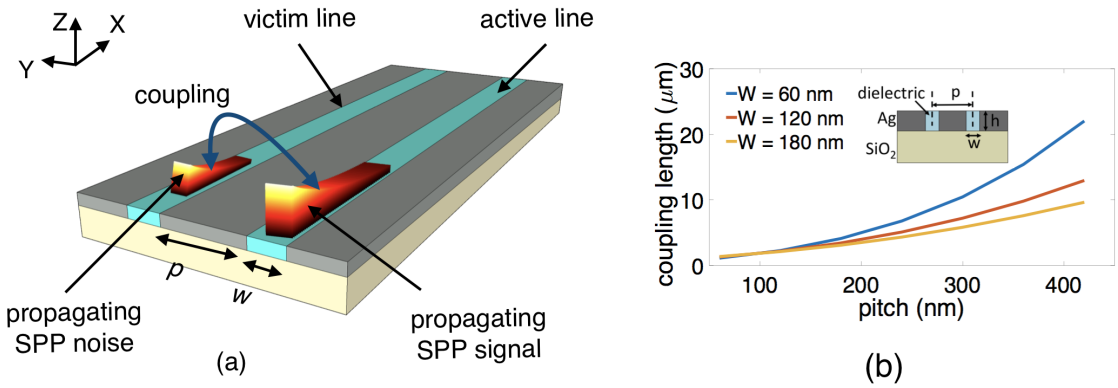

Figure 4.4: (a) Illustration of coupling between co-plane plasmonic wave gudies. (b) Plot showing coupling length L_p as a function of the waveguide pitch p for gap widths of 60, 120 and 180 nm, illustrating the trade-off between crosstalk and on-chip packing density.

waveguide is given by

$$L_c = \frac{\lambda_0}{\pi \Delta n} sin^{-1}\left(\sqrt{\frac{P_V}{P_A}}\right) \tag{4.15}$$

We calculate the length for 100% coupling of power as $L_{c,100\%} = \frac{\lambda_0}{2\Delta n}$. Figure 4.4(b) shows the coupling length L_c as a function of the waveguide pitch p for three different widths of the waveguide. While a larger pitch minimizes crosstalk, it puts a limitation on the on-chip footprint area and the achievable on-chip packing density which is another important figure-of-merit for us. Note that while the FOM graph in Figure 4.3(d) shifts towards the right for an increasing width of the waveguide illustrating an increase in the propagation length, the coupling length for a given pitch decreases with the increasing width of the waveguide as shown in Figure 4.4(b). This suggests the requirement of higher pitch for wider waveguides for minimizing crosstalk noise, thus increasing the footprint area and reducing the on-chip packing density.

4.5 Primitive Plamsonic Logic Gate

Next, we explore the two primitive logic gates required for wave-based computing: an inverter and a majority logic gate.

4.5.1 Interter Gate

An inverter gate can be designed by simply using a waveguide of length $(n+\frac{1}{2})\lambda$ as shown in Figure 4.5(a). Traveling a distance of $(n+\frac{1}{2})\lambda$, the phase of the output wave gets inverted from that at the input. Figure 4.5(b) shows the time-domain normalized integrated [1] electric field component E_Y at the input and output.

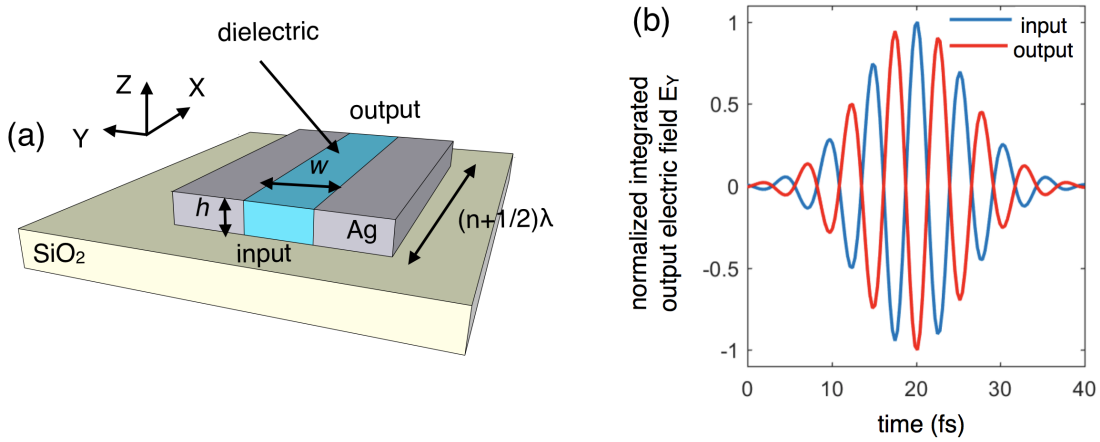

Figure 4.5: (a) Illustration of a plasmonic inverter logic gate. (b) Time-domain electric field component E_Y at the input and output, normalized to the total source electric field and integrated over the cross-section of the waveguide.

4.5.2 Majority Logic Gate

The functionality of a majority logic gate with N (odd) number of inputs is to return a true output if and only if more than half of its inputs (N/2) are true. A single stage 3-input plasmonic majority logic gate structure illustrated in Figures 4.6(a, b) has been investigated here. Table 4.2 lists the simulation parameters corresponding to Figure 4.6(a,b). It consists of three parallel input metal-slot waveguides where the SPPs are excited and a combiner region consisting of two bends where the SPPs merge into an output waveguide as shown schematically in Figure 4.6(b). The phase of the mode source is specified to be either 0^o

[1] the terms *normalized integrated* refers to averaging over the cross-section of the waveguide and normalization with respect to the total source electric field

Table 4.2: Simulation parameters for single-stage plasmonic majority gate

Parameter	Value	Units
Height (h)	100	nm
Input Waveguide Width (w)	60	nm
Output Waveguide Width (w)	120	nm *
Pitch (p)	360	nm
Merging Angle	35^o	nm
Length of Input/Output Waveguide (x_1)	200	nm
Length of Combiner Region (x_2)	500	nm
Excitation frequency (λ_0)	1.55	μm

* width increased to enhance transmission as explained later.

(from here on referred to as ϕ) or 180^o ($\phi + \pi$) for simulating a logic 1 or 0, respectively. Note that here we rely on the phase of the SPP wave as the computational or state variable. The effective refractive index of the injected SPP mode is calculated to be 1.79+0.0231i which results in a considerable range of usable propagation length of L_P = 5.31 μm (around 6 times the wavelength of the propagating SPP wave λ_{SPP} and 5 times the length of the majority gate $\sim$ 1 μm) and a sufficiently high degree of confinement of δ = 22 nm. The chosen dimensions corresponds to a coupling length L_C $\sim$ 10 μm. Since the coupling length L_C is almost an order of magnitude higher than the length of the majority gate ($\sim$ 1 μm), this choice of pitch size provides a good trade-off between crosstalk and on-chip packing density. The chosen dimensions in this work are comparable to that used by Pan, D. *et al.* [189] for MIM waveguides resulting in a similar propagation and coupling length. However, while the authors of ref. [189] relied on the intensity of the SPP wave for designing CMOS-oriented logic gates, here we utilize the phase of the SPP wave as the state variable to design majority logic gate.

Improving transmission through junction

As the three input waveguides inject power into a single output waveguide, a considerable backflow can occur due to reflection from the merging point. To improve transmission, we

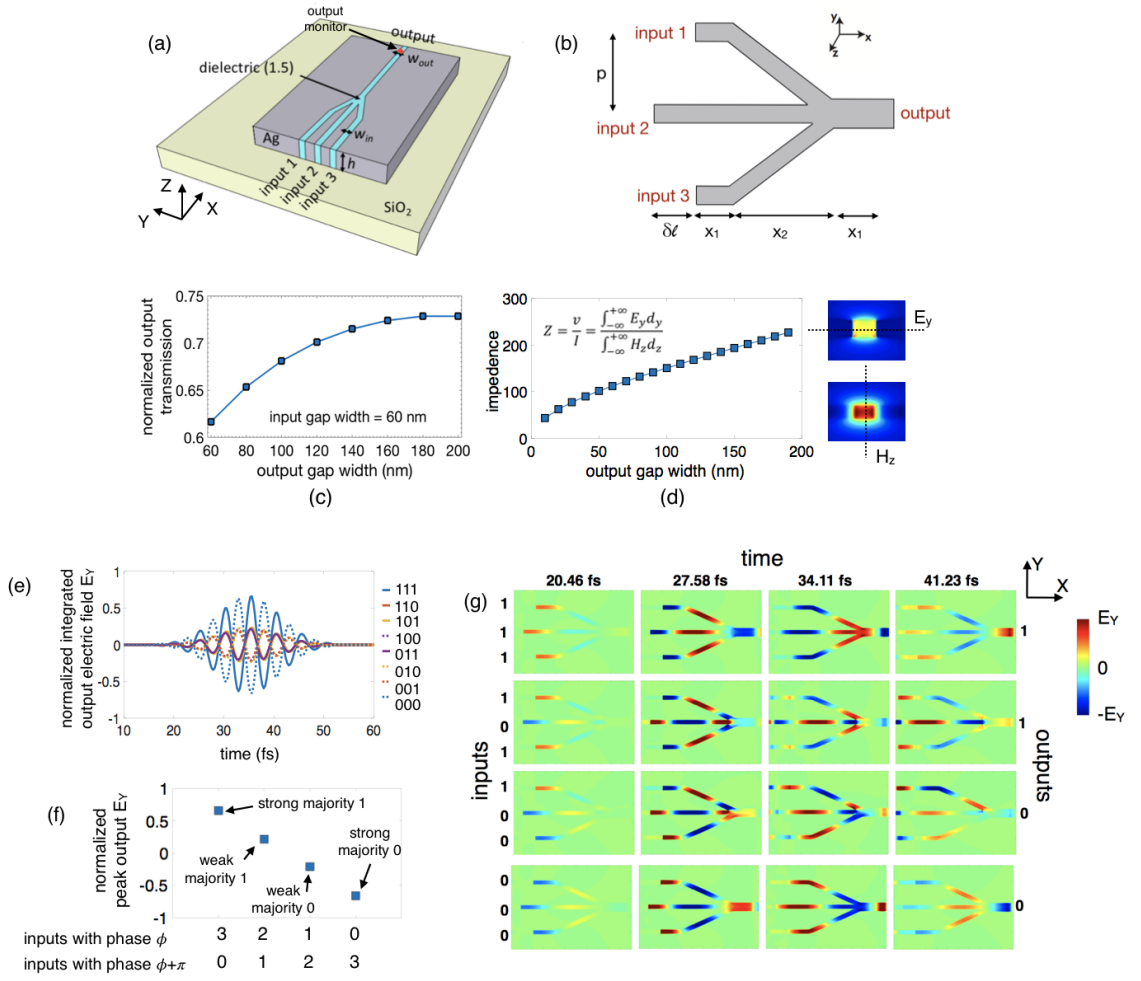

Figure 4.6: (a, b) Illustration of a single stage 3-input plasmonic majority logic gate. (c) Simulation result showing the increase in the normalized output transmitted power with the increase in the gap width of the output waveguide. (d) Calculated impedance of the waveguide as function of the gap width. (e) Simulation result for a 3-input plasmonic majority gate for 2^3 input combinations in terms of the time- domain electric field component E_Y at the output, normalized to the total source electric field and integrated over the cross-section of the output waveguide. (f) Calculated peak values of the normalized integrated electric field component EY at the output for different combinations of the input phases. (g) Time-lapse simulation results in terms of the distribution of E_Y in the x-y plane showing the propagation and interference of the SPP waves.

increase the gap width of the output waveguide. Figure 4.6(c) shows the increase in the transmitted output power (normalized to the source) through the 3-input junction with the increase in the gap width of the output waveguide. However, to avoid mode splitting and large increase in the required pitch for the next stage, we choose a moderately increased

output gap width of 120 nm. To better elucidate the result, we resort to an approach of impedance matching put forward by Cai et. al [217] which shows an increase in the transmission due to an increase in the impedance of the waveguide.

At wavelengths considerably larger than the size of the structure where the absorption is negligible (above the visible spectrum for silver), one can use the quasi-static approximation treating the waveguides as equivalent transmission lines with some characteristic impedance. Following the approach highlighted in [217] for 3-D waveguides, we calculate the direct integrals for the transverse electromagnetic fields to evaluate the effective voltage v and current I and hence the equivalent impedance Z

$$v = \int_{-\infty}^{+\infty} E_y d_y; \quad I = \int_{-\infty}^{+\infty} H_z d_z; \quad Z = v/I \tag{4.16}$$

Figure 4.6(d) illustrates the reason for the increase in the transmission.

Path length

The SPPs propagating through the two side arms of the majority gate have to cover an extra distance introduced by the bends. Since we rely purely on a constructive ($\Delta\phi$ = 0) or destructive interference ($\Delta\phi$ = π) between the input SPP waves, we need to compensate for the path difference δl between the middle and side arms and make all the three inputs equal in phase and strength. We introducing an extra path length of

$$\delta l = \frac{p}{sin[tan^{-1}\left(\frac{p}{x_2}\right)]} - x_2 \tag{4.17}$$

in the middle input waveguide. This can be done by shifting the excitation point to the left by δl as shown in Figure 4.6(b).

Figure 4.6(e) shows the numerical simulation result for a 3-input plasmonic majority gate for all 2^3 possible input combinations in terms of the time-domain electric field component E_Y at the output, integrated over the cross-section of the output waveguide and

normalized to the total source electric field and cross-sectional area of the output waveguide averaged over the yz-plane. The input logic combinations (1,1,1), (1,1,0), (1,0,1) and (0,1,1) which correspond to majority of the input being logic "1", i.e., SPP waves having a phase ϕ, result in logic "1" as the output, i.e., an output SPP wave having a phase ϕ. Similarly, the input combinations (0,0,0), (0,0,1), (0,1,0) and (1,0,0) result in an output SPP wave with phase $\phi + \pi$ depicting a logic "0" as the output. In addition to generating Boolean outputs, the proposed majority logic gate also has the capability to distinguish between a strong and a weak majority. As highlighted by the simulation results in Figure 4.62(e), an input logic combination of (1,1,1) corresponding to all the SPP waves having a phase ϕ, gives rise to maximum constructive interference resulting in a high amplitude output with the phase ϕ, i.e., a strong "1". On the other hand, for an input logic combination of (1,1,0), two of the SPP waves having phase ϕ and $\phi + \pi$ undergo destructive interference resulting in a low amplitude output with the phase ϕ, i.e., a weak logic "1". Figure 4.6(f) shows the peak values of the integrated electric field component E_Y at the output, normalized to the source electric field, for different combinations of the input phases. As can be seen, the output of a single stage 3-input majority gate has four different levels denoting a combination of Boolean output "1" and "0" and the strength of the majority. To further study the propagation and interference of SPP waves in the majority logic structure, we plot the time-lapse simulation results. Figure 4.6(g) shows the simulation results in terms of the distribution of the electric field component E_Y in the x-y plane at different snapshots in time for 4 different input combinations (1,1,1), (1,0,1), (1,0,0) and (0,0,0), depicting the propagation and interference of the SPP waves. The readers are referred to [218] for further details.

The majority gate also has the capability to perform "AND" and "OR" operation if one of the inputs is used as a control input. The set of logic primitives - inverter and majority, allow to effectively map most practical arithmetic functions, even when they cannot be directly matched well to just a cascaded majority logic structure. The multi-level output

of the majority gate depicts a combination of Boolean output "1" and "0" and the strength of the majority [218]. In order to utilize such a majority gate for Boolean computation, one needs to renormalize the output before feeding it to the next stage. However, here we strive to utilize this multi-level output to our advantage for non-Boolean computing. Since each of the stages in a cascaded structure (see Figures 4.7(a) or 4.9(a)) performs the dual functionality of Boolean output and strength of majority, the overall final result will display the Boolean logic output 1 or 0 and the overall strength the majority of all the inputs.

4.6 Cascadability

We analyze a 2-stage cascaded majority gate structure shown in Figure 4.7(a). The first stage comprises consists of three "3-input majority gates", each of whose outputs are combined in a majority gate fashion to form the second stage .

We use the same layout for the 3-input majority gate as seen in Figure 4.6(b) at each stage but with appropriate dimensional scaling as shown in Figure 4.7(b). The simulation parameters arre listed in Table 4.2. Note that due to the increase in the length of bends, the path difference (δl_1, δl_2 and δl_3) at each stage has to be considered separately and should be adjusted in the middle arm. For improved transmission via impedance matching, we choose the widths of the waveguides at each stage as w_1 = 60 nm, w_2 = 120 nm and w_3 = 180 nm. Note that we resort to a non-aggressive scaling of the widths since beyond 180 nm gap, the coupled MIM mode tends to split into two separate modes. However, we still gain from the fact that by increasing the widths, we increase the propagation length L_P of the SPP from 5.3 μm in the first stage to 8.46 μm in the second and 10.76 μm in the third. This proves to be beneficial since the overall size of the majority gate increases from one stage to the next.

In our numerical simulation, all the nine inputs are excited with the same stimulus in terms of source power and signal amplitude. The phase of the injected SPP waves are chosen to be either ϕ or $\phi + \pi$ representing logic "1" and "0", respectively. The final output

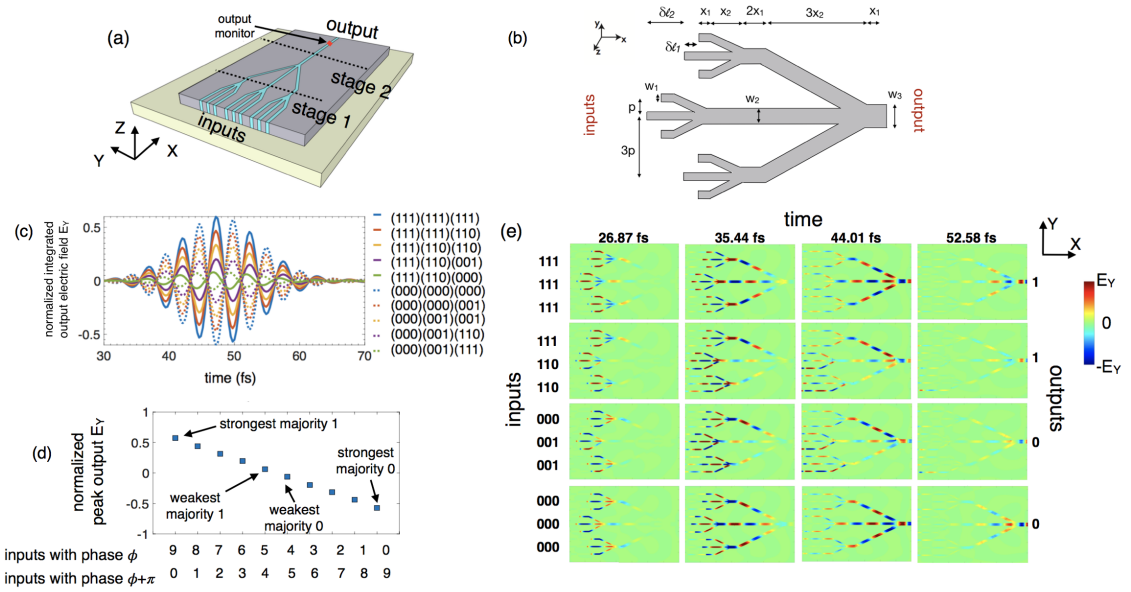

Figure 4.7: (a) Illustration of a 2-stage cascaded plasmonic majority logic gate. (b) Dimensional scaling and layout for cascaded majority gate structure. (c) Simulation results for the 10 representative input phase combinations in terms of the time-domain electric field component E_Y at the output, normalized to the total source electric field and integrated over the cross-section of the output waveguide. (d) Calculated peak values of the normalized integrated electric field component E_Y at the output for different combinations of the input phases. (e) Time- lapse simulation results in terms of the distribution of E_Y in the x-y plane showing the propagation and interference of the SPP waves.

is monitored at the end of the second stage as indicated in Figure 4.7(a). As mentioned earlier, the propagating SPP waves can be considered as exponentially decaying harmonic waves with the same frequency and amplitude and a certain phase shift relative to each other. The resultant output SPP wave due to wave interference can be written as $E_{out} = E_1 + E_2 + \cdots + E_8 + E_9 = E_0 e^{-k_y y} e^{i(k_x x - \omega t)} [e^{i_1} + e^{i_2} + \cdots + e^{i_8} + e^{i_9}]$, where i=1,$\cdots$,9 relates to the nine input waves.There are 2^9 possible input combinations for such a 2-stage cascaded majority logic gate; however, here we only concentrate on 10 representative cases as highlighted in Figures 4.7(c), (d) and (e) that capture all the possible combinations of input phases required for studying the cascaded majority gate structure.

Figure 4.7(c) shows the numerical simulation results for the 10 representative input combinations in terms of the time-domain normalized integrated average electric field com-

ponent E_Y at the output. For the case when all the inputs are logic "1", i.e., having the same phase ϕ, the resultant SPP wave $E_{out} = 9E_0 e^{-k_y y} e^{i(k_x x - \omega t + \phi)}$ has nine times the amplitude and phase ϕ resulting in a Boolean logic "1". In the extreme opposite case when all the inputs are logic "0", i.e., having the same phase $\phi + \pi$, the resultant SPP wave $E_{out} = -9E_0 e^{-k_y y} e^{i(k_x x - \omega t + \phi)}$ has nine times the amplitude but phase $\phi + \pi$ resulting in a Boolean logic "0". The peak amplitude of the output electric field depends on the number of inputs with phases ϕ (m) and $\phi + \pi$ (n) and varies as $E_{out}^{peak} = (m - n)E_0$ as seen in Figures 4.7(c, d). Overall, we obtain 10 different levels of output amplitude of the electric field component E_Y, each corresponding to the strength of the majority of the input. The strongest majorities where all the 9 inputs have the same phase ϕ or $\phi + \pi$ produce the highest output amplitude with opposite sign as indicated in Figure 4.7(d). Likewise, the weakest majorities where only 5 inputs have phase ϕ while the remaining 4 have phase $\phi + \pi$ or vice-versa produce the lowest magnitude of output amplitude. The time-lapse simulation results in terms of the distribution of the electric field component E_Y in the x-y plane for 4 representative input combinations (111,111,111), (111,110,110), (000,001,001) and (000,000,000) are shown in Figure 4.7(e). The readers are referred to [218] for further details.

4.7 Referencing Technique for Detection

As mentioned earlier, the binary data is encoded in the phase of the excited SPP wave (phase ϕ representing logic "1" and phase $\phi + \pi$ representing logic "0") which we use as the state variable for computing. Hence, after wave interference, the relevant parameter to extract is the phase of the output SPP wave which gives the Boolean output of "1" or "0". However, it may be challenging to devise a precise THz phase-detection scheme for our plasmonic logic gate operating at 193 THz (see dispersion plot in Figure 4.3(b)). In addition, our proposed plasmonic majority gate also displays a non-Boolean characteristic in terms of indicating the strength of the majority which further adds to the expressive

power of the plasmonic majority gate. As such, in this work, we propose a novel approach to extract both the amplitude and phase information from the output by using a referencing technique. An illustration for using the referencing technique at the end of the 2-stage cascaded structure is shown in Figure 4.8(a). In addition to the 9 input SPP wavess, we also inject a reference signal E_{ref} that merges at the output of the second stage. We choose the gap width of the reference waveguide to be $3w$. We adjust the amplitude and the phase of the injected reference signal $E_{ref} \approx 9E_0 e^{-k_y y} e^{i(k_x x - \omega t + \phi)}$ to match the output of the cascaded gate for the case of the strongest majority logic "1" (the case of all inputs 1 in Figure 4.7(c)). This can be done by using higher excitation power for the reference source and accounting for the total path delay for the reference signal.

Figure 4.8(b) shows the numerical simulation result for the 2-stage cascaded majority with reference for the 10 representative input combinations in terms of the time-domain normalized average integrated electric field component E_Y at the output. Since the reference signal has been adjusted to have a phase ϕ, all the input combinations having majority of the input as logic "1", i.e., SPP waves having a phase ϕ, result in a constructive interference while all majority "0" cases having phase $\phi + \pi$ result in destructive interference. However, since we set the peak amplitude of the reference signal to be $E_{ref}^{peak} \geq 9E_0$ higher than all the other 9 inputs, we get a Boolean output of logic "1" for all the 10 cases (output SPP waves having phase ϕ), but with varying levels of output amplitude of the electric field component E_Y as indicated in Figure 4.8(b) and (c). In contrast to Figure 4.7(c) and (d), in this case the strongest majority with 9 inputs having phase ϕ produces the highest magnitude of output electric field E_Y while the strongest majority with 9 inputs having phase $\phi + \pi$ produces the lowest magnitude of output E_Y as indicated in Figure 4.8(c). Thus, the referencing technique directly translates the information encoded in the amplitude and phase of the output SPP wave into the intensity of the output electric field as illustrated in fFigure 4.8(c). We can further define the peak amplitude of the output electric field or the output power transmitted for the case when only the reference signal is present as the

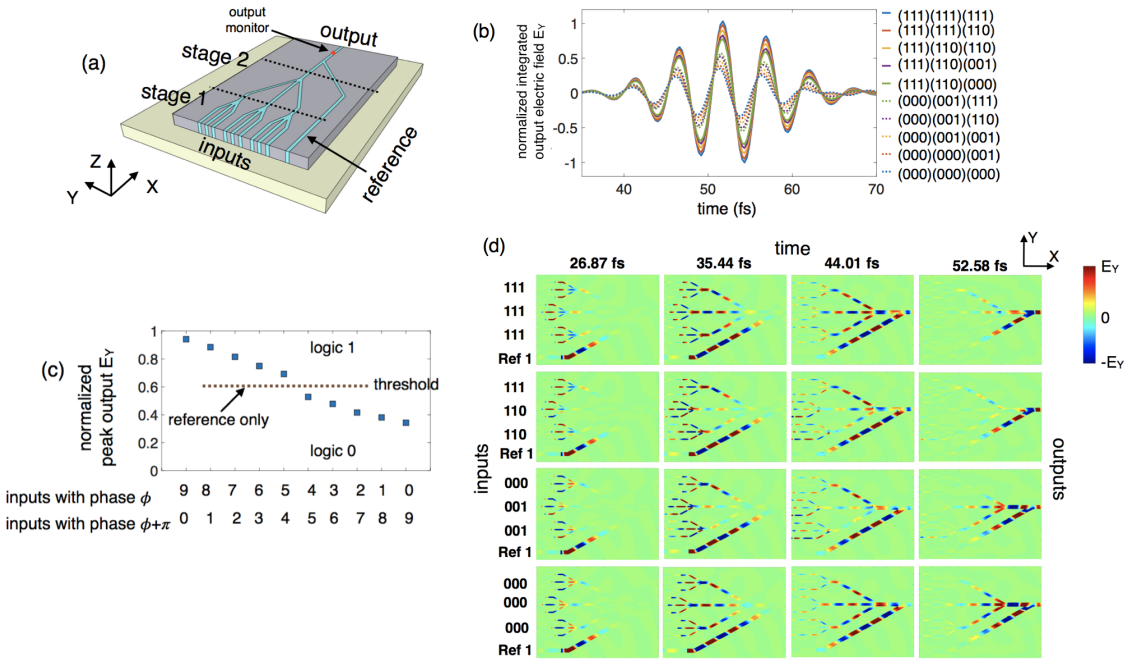

Figure 4.8: (a) Illustration of a 2-stage cascaded plasmonic majority logic gate with the reference signal. (b) Simulation results for the 10 representative input phase combinations in terms of the time-domain electric field component E_Y at the output, normalized to the total source electric field and integrated over the cross-section of the output waveguide. (c) Calculated peak values of the normalized integrated electric field component E_Y at the output for different combinations of the input phases. The peak amplitude of the output electric field in (c) for the case when only the reference signal is present is defined as the threshold level. (d) Time-lapse simulation results in terms of the distribution of E_Y in the x-y plane showing the propagation and interference of the SPP waves.

threshold level. As such, anything above the defined threshold can be considered as a logic "1" while anything below gives a logic "0". Figure 4.8(d) shows the time-lapse simulation results in terms of the distribution of the electric field component E_Y in the x-y plane for 4 representative input combinations (111,111,111), (111,110,110), (000,001,001) and (000,000,000), depicting the propagation and interference of the SPP waves along with the reference signal. The readers are referred to [218] for further details.

4.8 Limit on the Number of Cascadable Stages

While it is highly desired to have a multi-staged cascaded plasmonic logic without intermediary signal conversion between plasmon and charge domain, the propagation loss of SPP puts a limitation on the feasible number of cascaded stages. As shown in Figure 4.9(a), the size of majority logic gate increases with the number of stages from an estimated value of 0.636 μm^2 for the first stage to 4.66 μm^2 and 38.24 μm^2 for the second and third stage, respectively. The increase in the path-length traveled by the SPP compared to the propagation length L_P increases the transmission loss from around 30$\%$ in the first stage to more than 50$\%$ in the third stage. Hence, we anticipate that it may be inefficient to go beyond the third stage without using either amplifiers to boost the signal amplitude or convert plasmonic signal to voltage signal at the end of the third stage [218]. An additional constraint comes from distinction or separation between output levels after referencing. The number of output levels (amplitude of electric field E_Y or transmitted power) increases with the number of stages and input, from 4 in 1st stage to 10 in the 2nd and so on. Figure 4.9(b) shows the range of amplitude of the output electric field E_Y for logic "1" and "0" obtained at the end of each stage. Note that the range of output for both logic "1" and "0" decreases due the propagation loss from one stage to the next. Hence, even though the referencing technique will translate the information encoded in the amplitude and phase of the output SPP wave into electric field intensity, it will be difficult to separate or distinguish between the output levels for values of logic "1" and "0" as they get closer to the threshold level (case of weakest majority). We further investigate the possibility of separation of states above and below the threshold level (corresponding to logic "1" and "0") by plotting the resolution as a function of the number of stages shown in Figure 4.9(c). We define the resolution as the difference between the minimum value of peak output E_Y for logic "1" and the maximum value of peak output E_Y for logic "0" (case of weakest majority outputs),

$$resolution = \Delta E_{Y,out} = E_{Y,min}^{logic1} - E_{Y,max}^{logic0} \tag{4.18}$$

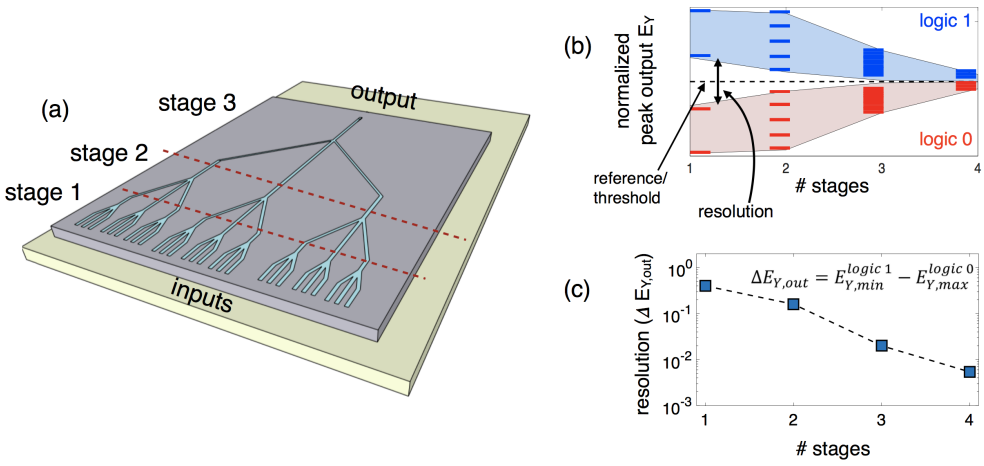

Figure 4.9: (a) Illustration of a multi-stage cascaded plasmonic majority logic. (b) Plot showing the range of amplitude of the output electric field E_Y for logic "1" and "0" obtained at the end of each stage. The range of output decreases due to propagation loss at each stage. (c) Resolution, defined as the difference between the minimum value of peak output E_Y for logic "1" and the maximum value of peak output E_Y for logic "0" (case of weakest majority outputs), as a function of the number of stages.

4.9 Non-Boolean Computing with plasmonics

Due to high throughput, the proposed cascaded plasmonic majority gate can be of great use in highly parallel real-time signal and data processing applications [218]. One good illustration of this usage is present in the non-boolean decision making process of a pattern recognition system. The non-boolean decision making process involves counting the number of matches and mismatches and determining the degree of match or mismatch between the input and the reference pattern. We believe the proposed cascadable plasmonic majority logic gate can find a direct utility here. The patterns can be considered as binary valued matrices with black and white pixels represented as logic "1" and "0", respectively. Using the majority voting capability of the gate along with the referencing technique, it would be possible to count the number of match or mismatch at each stage with the final output portraying an overall match or mismatch between the input and the reference pattern and the degree of match or mismatch found.

CHAPTER 5

SPINTRONIC INTERCONNECT USING SKYRMIONS

5.1 Background

5.1.1 Skyrmion - A General Concept

The name *"skyrmion"* is derived from the nuclear physicts Tony Skyrme who, in 1962, developed a nonlinear field theory for interacting pions and concluded that topologically stable field configurations, aka. skyrmions, occur as particle-like solutions [219]. Since the original prediction of Tony Skyrme, skyrmions have been considered as a generalized mathematical object in various field of physics. Skyrmions have been predicted to occur in quantum Hall magnets [220–222], ferromagnetic Bose-Einstein condensates [223, 224] and liquid crystals [225, 226]. Around 1990s, Bogdanov et. al. [227–229] theoretically showed that localized spin textures (skyrmions) also occur as mean-field ground state for non-centrosymmetric magnetic materials where they are stabilized by chiral spin-orbit interactions, thereby defying Derricks scaling arguments [230] regarding instability of solitons in a standard Ginzburg-Landau functional.

5.1.2 Magnetic Skyrmions

Magnetic skyrmions are chiral spin structures displaying a whirling configuration as shown in Figure 5.1(a,b). Following the pioneering work of A. N. Bogdanov [227–229] including the prediction of chiral skyrmions in B20-type helimagnets [231] in 2006, Muehlbauer et al. in 2009 first experimentally observed magnetic skyrmions in B20-type chiral material MnSi using small-angle neutron scattering [232]. Since then, magnetic skyrmions have been the focus of intense research in a variety of non-centrosymmetric magnetic materials like MnSi [233, 234] (see Figure 5.1(c)), FeCoSi [235], FeGe [236] and MnFeGe [237] and in

multilayers of heavy metals exhibiting high spin-orbit coupling and ultrathin magnetic films with broken inversion symmetry like Ir/Fe [238], Pt/CoFe [239], Ta/CoFe [240],Pt/Co/Ta [240], Pt/Co/Ir [241], Pt/CoFeB/MgO [240], Ta/CoFeB/TaOx [242] and Ta/CoFeB/MgO [243].

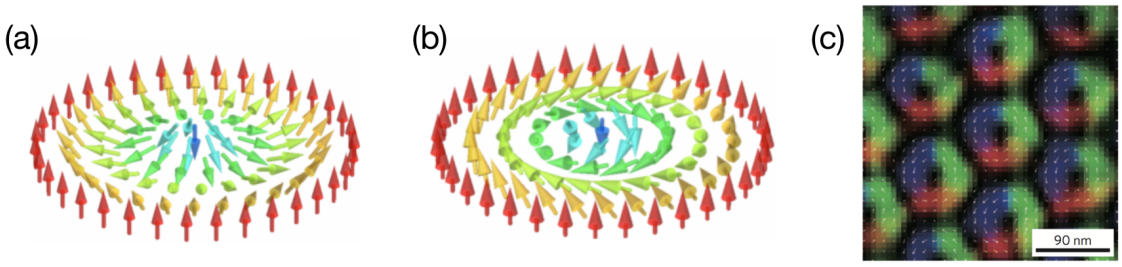

Figure 5.1: Spin configurations in (a) Bloch and (b) Neel type skyrmions. (c) Lorentz microscopy image of a skyrmion lattice in $Fe_{1x}Co_xSi$. Adapted from [234]

The spin profile of a skyrmion can be described as [244]

$$\vec{m}(\vec{r}) = [sin(\theta(\vec{r})cos(m\phi + \gamma), sin(\theta(\vec{r})sin(m\phi + \gamma), cos(\theta(\vec{r})] \tag{5.1}$$

where $\theta(\vec{r})$ is the radial function defining the z-component (out-of-plane) of the magnetization. The numbers m and γ represent the vorticity[1] and helicity of the skyrmion, respectively, and are used to classify the skyrmion type. The whirling spin configuration of a skyrmion is characterized by the topological skyrmion number or the winding number defined as [244]

$$S = \frac{1}{4\pi} \int \int \vec{m} \cdot \left(\frac{\partial \vec{m}}{\partial x} \times \frac{\partial \vec{m}}{\partial y} \right) dxdy \tag{5.2}$$

and is determined by the product of the vorticity and the difference between the spin direction of the core and the periphery of the skyrmion. The helicity does not directly contribute to the skyrmion number, but is determined by the type of DMI which in turn defines the type of skyrmion. For example, m = 1 represents a skyrmion with S = -1 and m = -1 represents an anti-skyrmion with S = 1. With m =1, a helicity of γ = 0 and π then represents

[1]The vorticity defines the winding of the spin configuration projected onto the x-y plane

a Bloch-type or Neel-type skyrmion, respectively [244] as shown in Figure 5.1(a,b).

5.1.3 Magnetic Skyrmions for Beyond-CMOS technology: Prior Work and Challenges

Recently, information processing utilizing magnetic quasi-particles such as magnons, domain walls and skyrmions has been the focus of intense research for low-power, non-volatile beyond-CMOS logic, memory and interconnect applications. The advantages of utilizing magnetic skyrmions for information processing stems from their topological stability [244], smaller size [245–247], compared to magnetic bubbles stabilized by magnetostatic interaction, and motion induced by current densities as low as 10^6 A/m^2, see [233, 246, 248–250]. This has led to a flurry of research on the development of a dense, low-power skyrmion-based racetrack memory [240, 243, 246, 251, 252], similar to the domain-wall racetrack memory [253] proposed earlier by IBM. Besides showing promise in memory technology, recent works have also highlighted the development of skyrmion-based nano-oscillator [254], logic gate [255], transistor [256] and reservoir computing [257].

However, the potential of skyrmions in connecting magnetic logic remains unexplored. Relying on the small size, high-packing density, displacement via ultra-low current density, and robustness to defects and pinning, it is anticipated that a skyrmion-based magnetic interconnect can provide a low-power, high throughput and robust alternative to other candidates for interconnecting magnetic logic using spin drift-diffusion mechanism [258, 259], automotion of domain wall [260], spin waves or an electrical transduction for charge to spin signal conversion [261]. As essential requirement of skyrmion-interconnect is to decouple the writing and driving mechanism. Figure 5.2 shows an shows an illustration of a possible implementation of skyrmion interconnect used for connecting magnetic logic (which can be a traditional all-spin-logic (ASL) [58], modified magnetostriction-assisted ASL [262] or spin wave logic device [57]). As shown in Figure 5.2, the last stage of the magnetic logic can be connected to the skyrmion interconnect using a conventional spin valve (CSV) structure. Depending on the orientation of the ferromagnetic layer (last stage

of the magnetic logic), spin current with polarization $\sigma_{spin} = +z$ or $-z$ can be injected into the magnetic layer of the skyrmion interconnect. A $+z$ polarized spin current retains the uniform ferromagnetic state of the nanowire while a $-z$ polarized spin current aids in the nucleation of a magnetic skyrmion. Hence, the stream of binary data (sequence of "1"s and "0"s) can be represented as the presence or absence of a skyrmion. Once created, the skyrmions can then be moved along the ferromagnetic nanowire using spin-orbit torque by injecting a charge current through the heavy metal below.

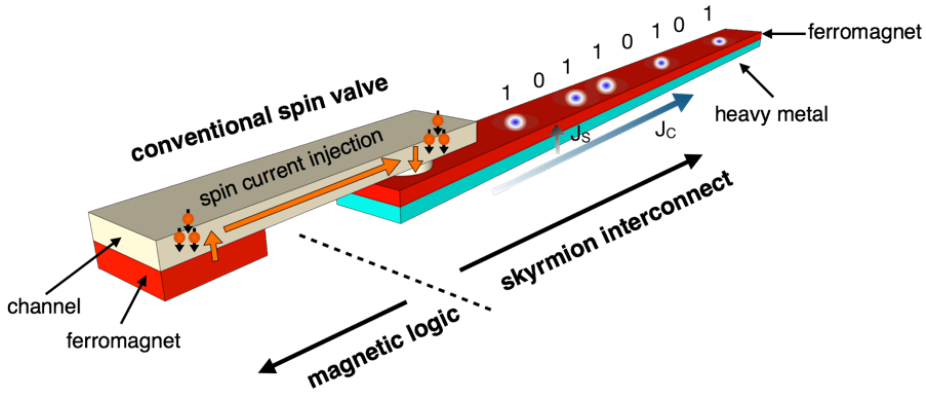

Figure 5.2: Illustration of a possible implementation of skyrmion interconnect used for connecting a magnetic logic. The orientation of the ferromagnetic layer (last stage of the magnetic logic) will dictate the polarization of the injected spin current that can nucleate a magnetic skyrmion. The stream of binary data (sequence of "1"s and "0"s) is represented as the presence or absence of a skyrmion in the interconnect.

Several techniques have been proposed for skyrmion nucleation till now [242, 243, 245, 246, 250, 263–265]. However, they either require low temperature [245], provide an uncontrollable random production of skyrmion bubbles [242, 266, 267] at available DMI, require a considerably large DMI for robust transformation of domain wall to skyrmions [265, 268] or require engineered interfacial perpendicular magnetic anisotropy [243]. An earlier proposal by Iwasaki et al. [250] and recent demonstrations by Buttner et al. [264] and Everschor et al. [263] have provided alternative controlled and integrated methods of skyrmion nucleation using an electric current. However, they utilize the same stimulus (electric current) for skyrmion nucleation and dynamics, relying on the magnitude of the applied current pulse to either write or move skyrmions, and as such are mostly suited for

a skyrmion-based racetrack memory technology.

5.1.4 Overview of Chapter

The focus of this chapter is to develop a low-power, high throughput, robust skyrmion-based interconnect for magnetic logic. The chapter has been primarily divided into three parts, each dedicated to the three essential ingredients for any interconnect technology: (a) write data, (b) transport data and (c) read-out data. The first part discusses the stability of an isolated skyrmion (Section 5.2) considering the dynamic interplay between the various microscopic phenomena involved, and the skyrmion nucleation process (Section 5.3). A "localized spin current injection" based nucleation technique has been adapted that allows decoupling the writing from the driving mechanism and provides a generalized and universal scheme for skyrmion creation in materials with low chirality. The robustness of the nucleation scheme has also been discussed. In the second part of this chapter, the idea of using skyrmions for interconnecting magnetic logic has been investigated. Section 5.4 describes the spin-orbit-torque driven skyrmion dynamics. Skyrmions can be packed with less than 100 nm spacing giving rise to closely packed interconnects, which has been discussed in Section 5.5. Section 5.6 briefly discusses the prospective methods for skyrmion detection, however, a detailed analysis remains beyond the scope of this research. Finally, the performance of skyrmion interconnects has been discussed in Section 5.7 and compared to other spintronic interconnects.

5.2 Stabilizing Skyrmions

The stabilization of magnetic skyrmions depends on the dynamic interplay between the various microscopic phenomena explained below [244].

Long-ranged magnetic dipolar interactions

While the perpendicular magnetic anisotropy (PMA) in thin films prefer out-of-plane magnetic configuration, the dipolar interaction (otherwise known as shape anisotropy) dictates the magnetization to stay in-plane. The competition between the two gives rise to periodic stripe domains and magnetic bubble skyrmions. The size of the bubble skyrmions are typically of the order of 0.1-1 μm, comparable to the spiral period determined by the ratio of the dipolar and exchange interactions.

Relativistic Dzyaloshinskii-Moriya interaction (DMI)

This chiral anti-symmetric exchange interaction [269, 270] is induced due to the lack or breaking of inversion symmetry in lattices or at the interface of a magnetic film and a heavy metal exhibiting strong spin-orbit coupling. The generalized DMI interaction between two neighboring atomic spins $\vec{S_1}$ and $\vec{S_2}$ is defined as

$$\mathcal{H}_{DMI} = -\vec{D}_{12} \cdot \left(\vec{S_1} \times \vec{S_2}\right). \tag{5.3}$$

where $\vec{D}_{12}$ is the DM vector. Contrary to the ferromagnetic exchange interaction that favors collinear arrangement of spins, DMI allows the stabilization of helical magnetic order. In B20-type materials, the bulk DMI takes the form

$$\mathcal{H}_{DMI} = D\vec{m}(\vec{r}) \cdot \left[\vec{\bigtriangledown} \times \vec{m}(\vec{r})\right] \tag{5.4}$$

and supports Bloch-type skyrmions, where $\vec{m}(\vec{r})$ describes the local magentic moment. The interfacial DMI has been predicted to arise due to a *"3-site indirect exchange mechanism"* [271] between two neighboring atomic spins $\vec{S_1}$ and $\vec{S_2}$ with a neighboring atom of a heavy

metal possessing large spin-orbit coupling. In this case, the interfacial DMI takes the form

$$\mathcal{H}_{DMI} = D\big[m_z(\vec{r})\vec{\bigtriangledown}\cdot\vec{m}(\vec{r}) - \big(\vec{m}(\vec{r})\cdot\vec{\bigtriangledown}\big)m_z(\vec{r}) \tag{5.5}$$

DMI stabilized skyrmions typically have sizes in the 10-100 nm range.

Two other interactions (frustrated exchange interactions [272] and four-spin exchange interactions [238]) result in skyrmion sizes of the order of the lattice constant ($\sim$1 nm) and are under the focus of intense research nowadays. For the rest of this chapter, we focus on isolated skyrmions stabilized by the dipolar, anisotropy (PMA), Heisenberg exchange and interfacial DMI interactions.

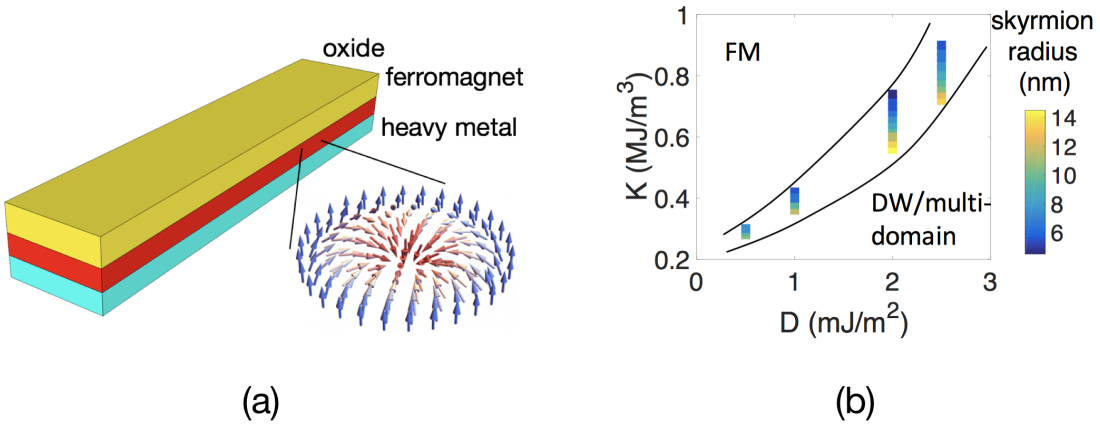

Figure 5.3: (a) Multilayer stack of ferromagnetic layer sandwiched between a heavy metal exhibiting high spin-orbit coupling and an oxide layer hosting a Neel skyrmion. (b) Skyrmion stability for different values of DMI (D) and PMA (K). The color map shows the radius of the stabilized skyrmion.

We consider a multilayer stack of ferromagnetic layer sandwiched between a heavy metal exhibiting high spin-orbit coupling and an oxide layer as shown in Figure 5.3(a). The interface between the heavy metal and the ferromagnet generates an interfacial DMI. Additionally, such a multilayer also displays a strong perpendicular magnetic anisotropy (PMA). While a higher value of DMI is sought for, recent experimental investigations have suggested a maximum obtainable value of 2 mJ/m^2 and 4 mJ/m^2 for Ir/Co/Pt [273]

Table 5.1: Simulation parameters for skyrmion stability and nucleation.

Parameter	Value	Units
Width of nanowire	60	nm
Thickness of nanowire	1	nm
Saturation magnetization (M_S)	650	kA/m
Exchange Stiffness (A)	10	pJ/m
DMI (D)	0.5 - 3	mJ/m^2 *
PMA (K)	0.26 - 0.9	MJ/m^3 *

* the chosen combinations of D and K stabilizes skyrmion with diameter 20 - 30 nm.

and Ir/Fe [238] systems, respectively. In more beyond-CMOS technologically relevant spintronic materials like Pt/CoFeB [240, 264] and Ta/CoFeB [242, 274], the obtained DMI is 1-1.5 and 0.1-0.5 mJ/m^2, respectively.

We choose the ferromagnetic material parameters corresponding to ultrathin CoFeB while the DMI strength is varied between 0.5 - 3 mJ/m^2 (that corresponds to a choice of Pt, Ta and Ir as the heavy metal). The simulation parameters are listed in Table 5.1. Since the stabilization of an isolated skyrmion depends on the interplay between the dipolar, exchange, DMI and anisotropy energy, we correspondingly vary the perpendicular anisotropy K between 0.26 - 0.9 MJ/m^3 as shown in Figure 5.3. For a given K, the skyrmion size increases with increasing DMI (till the critical value $D_C = \frac{4}{\pi}\sqrt{AK_{eff}}$), where K_{eff} is the effective out of plane anisotropy, while for a fixed DMI, increasing K reduces the skyrmion diameter. For the rest of our simulations, we chose the combination of D and K values to be (0.5 mJ/m^2, 0.26 MJ/m^3), (1.0 mJ/m^2, 0.35 MJ/m^3), (1.5 mJ/m^2, 0.45 MJ/m^3), (2.0 mJ/m^2, 0.6 MJ/m^3), (2.5 mJ/m^2, 0.8 MJ/m^3) and (3.0 mJ/m^2, 0.9 MJ/m^3) that correspond to a skyrmion diameter of 20 - 30 nm.

5.3 Nucleating Isolated Skyrmion

5.3.1 Spin-Current Injected Nucleation Mechanism

We revisit the process of skyrmion nucleation proposed by Sampaio et al. [246] in an ultrathin narrow nanowire geometry as shown in Figure 5.4(a). We consider a spin current injection through a circular nano-contact as shown in Figure 5.4(a) for skyrmion nucleation. The nanowire is initially magnetized ($\vec{m}_{FM}$) in the +z direction. The spin current with spin polarization ($\vec{\sigma}_{spin}$) in the -z direction is injected through the circular nano-contact region of diameter 20 nm for a time period of 1 ns. Throughout this work, the field-like torque is assumed to be 0; however, including the field-like torque in simulations does not change the main conclusion of the work. At low spin current density (J_S), no domain reversal is observed and the initial ferromagnetic state is retained. Above a critical threshold ($J_S \geq 1.5 \times 10^{12}$ A/m^2), we see the formation of a reversed magnetic domain. However, the possibility for a successful skyrmion nucleation depends highly on the strength of the DMI as depicted in Figure 5.4(b). This observation is consistent with the simulation results by Sampaio et al. [246] where such a skyrmion nucleation using spin injection has been successfully achieved in the presence of a high DMI value ($D \geq 5$ mJ/m^2 in their simulation). Other simulation works involving such nucleation technique have also considered a material system with a high DMI value of D = 3 mJ/m^2 [275, 276]. Here, a controlled single skyrmion nucleation mechanism in a confined nanowire geometry with sub-100 nm width has been investigated with material systems (Pt/CoFeB or Ta/CoFeB) displaying a lower DMI (< 2 mJ/m^2).

To better elucidate the reason behind the two distinct regions of success and failure shown in Figure 5.4(b), the skyrmion nucleation mechanism has been investigated in details. The pathway towards a successful skyrmion nucleation using this technique involves: (a) creation of a magnetic domain with reversed magnetization surrounded by a pseudo-domain wall containing one or more pairs of vertical Bloch lines (VBLs), (b) eventual

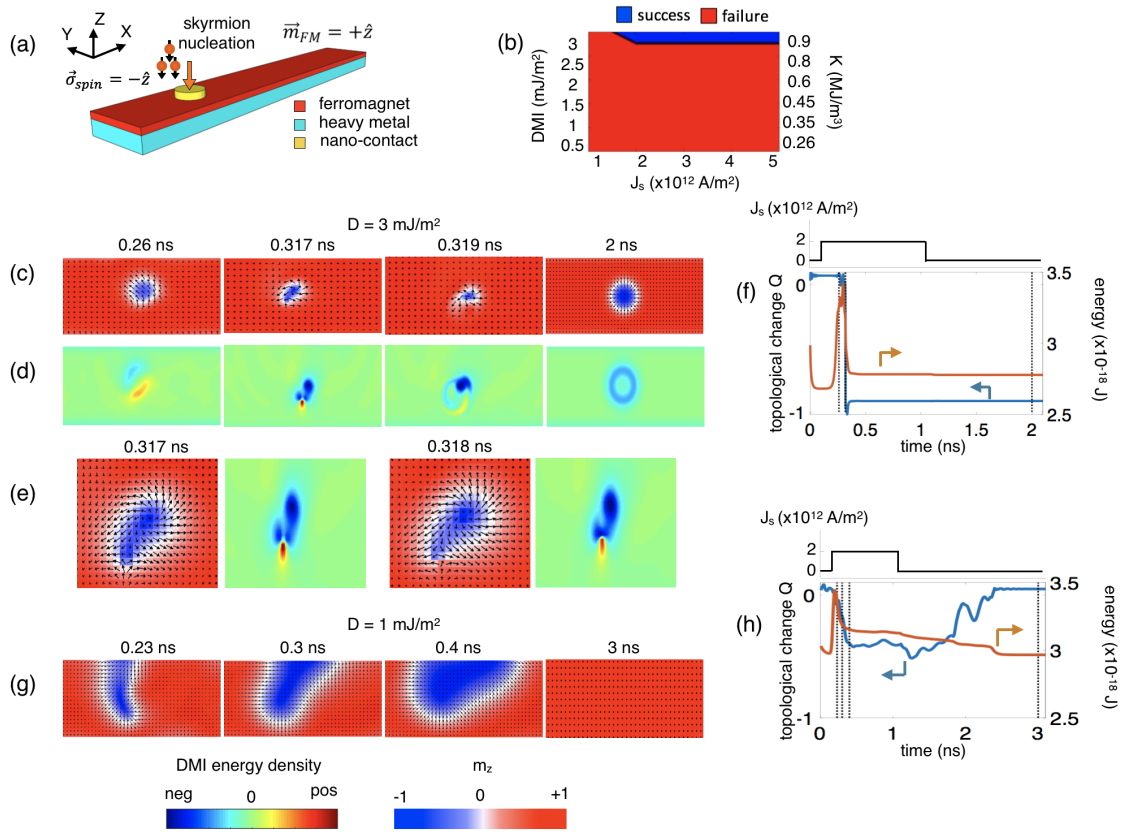

Figure 5.4: (a) Scheme of skyrmion nucleation using localized spin current injection into an ultrathin ferromagnetic nanowire sandwiched between a heavy metal and an oxide. The spin-polarized current is injected through a circular nano-contact. (b) Probability of skyrmion nucleation for different values of (D, K) and injected spin current density J_s. (c, d) Temporal evolution of magnetization and corresponding DMI energy density after spin current injection for D = 3 mJ/m^2. (e) Zoom-in of the spin current injection region showing a large positive DMI energy density concentrated within a small defect-like region that leads to the annihilation of VBLs and generation of skyrmion. (f) Change in the skyrmion number S from 0 to -1 upon VBL annihilation and the change in the total energy overcoming the topological barrier. (g) Temporal evolution of magnetization after spin current injection for D = 1 mJ/m^2. (h) Corresponding change in the skyrmion number and the total energy.

annihilation of the VBLs creating a magnetic bubble with defect-free domain wall and (c) relaxation of the magnetic bubble into a circular skyrmion structure. As shown in Figure 5.4(c) for the case of large DMI (3 mJ/m^2) and injected spin current density $J_S = 2 \times 10^{12}$ A/m^2, at t = 0.26 ns, the magnetization inside the nano-contact region is reversed with magnetization pointing in the -z direction. This magnetic configuration corresponds to a mag-

netic bubble surrounded by a pseudo-domain wall. The pseudo-domain wall is composed of two regions with opposite chirality (left-handed with spins pointing outward and right-handed with spins pointing inward) separated via a pair of vertical Bloch lines (VBLs). The corresponding distribution of DMI energy density is shown in Figure 5.4(d). As the spins inside the pseudo-domain wall reorient rapidly, the region with chirality favored by DMI (left-handed in our case) expands while the region with opposite chirality shrinks into a small defect-like region trapping a large positive DMI energy density as shown at t = 0.317 and 318 ns in Figure 5.4(c, d, e). As the size of this defect-like region similar to a Bloch point rapidly decreases, eventually the large positive DMI energy density forces the VBLs to get annihilated with rapid reorientation of the spins and emission of radial spin waves as seen at t = 0.319 ns in Figure 5.4(c, d). The emission of the spin waves carries off energy that ultimately explains the stability of the skyrmion through the creation of the potential well necessary for skyrmion stability and will be the subject of a separate work. Figure 5.4(f) shows the change in the total energy of the system, overcoming the topological energy barrier. As the VBLs get annihilated, the skyrmion number drastically changes from 0 to a value close to -1 corresponding to an isolated magnetic skyrmion as shown in Figure 5.4(f).

The case of a lower DMI (1 mJ/m^2) presents a different scenario. As shown in Figure 5.4(g), upon spin current injection, VBLs are created. However, as the spins inside the pseudo-domain walls reorient in the direction favored by the DMI, the VBLs get attracted towards the edge of the nanowire due to the attractive interaction with the inward tilted edge magnetization as seen at t = 0.23 in Figure 5.4(g). Eventually, the VBLs are expelled and the magnetic bubble transforms into an edge-to-edge domain wall that slowly expands to form a multi-domain state as seen at t = 0.3 and 0.4 ns. As the current pulse stops after 1 ns, the domain wall collapses to form the initial uniform ferromagnetic state. Figure 5.4(h) shows the change in the total energy density and the skyrmion number.

Table 5.2: Parameters for edge material.

Parameter	Value	Units
Saturation magnetization (M_S)	840	kA/m *
Exchange Stiffness (A)	12	pJ/m *
DMI (D)	0.1	mJ/m^2 *
PMA (K)	5 - 17	MJ/m^3 *

* adapted from [277].

5.3.2 Edge Material for Confinement

To circumvent the problem of VBLs getting attracted towards the edge giving rise to domain wall formation, next we incorporate an additional potential barrier at the two edges of the nanowire as shown in Figure 5.5(a) using a 5 nm wide edge material with high PMA. As an illustrative example, we consider the material parameters for the edge material equal to that of Samarium Cobalt $SmCo_5$, see Table 5.2 for material parameters. Similar to the previous case, the nanowire initially has a uniform magnetization in the +z direction while the spin current with spins polarized in the -z direction is injected through the circular nano-contact region of diameter 30 nm for 1 ns long. We mainly focus on the range of DMI that previously resulted in an unsuccessful skyrmion nucleation owing to the formation of edge-to-edge domain wall. As shown in Figure 5.5(b), we can now successfully nucleate skyrmions with lower DMI (< 3 mJ/m^2) owning to the presence of the edge material. However, the required spin current density remains high. Figure 5.5(c) shows the skyrmion nucleation mechanism with injected spin current density $J_S = 10 \times 10^{12}$ A/m^2 in the presence of a DMI of 2 mJ/m^2. The pathway for successful skyrmion nucleation remains the same as before. At t = 0.12 ns, the magnetization inside the nano-contact region is reversed forming a magnetic bubble surrounded by a pseudo-domain wall containing a pair of VBLs. The repulsive force from the edges with high PMA prevents the VBL from getting expelled at the edge of the nanowire. The spins inside the pseudo-domain wall rapidly reorient at t = 0.15 ns as seen in Figure 5.5(c) expanding the region with chirality

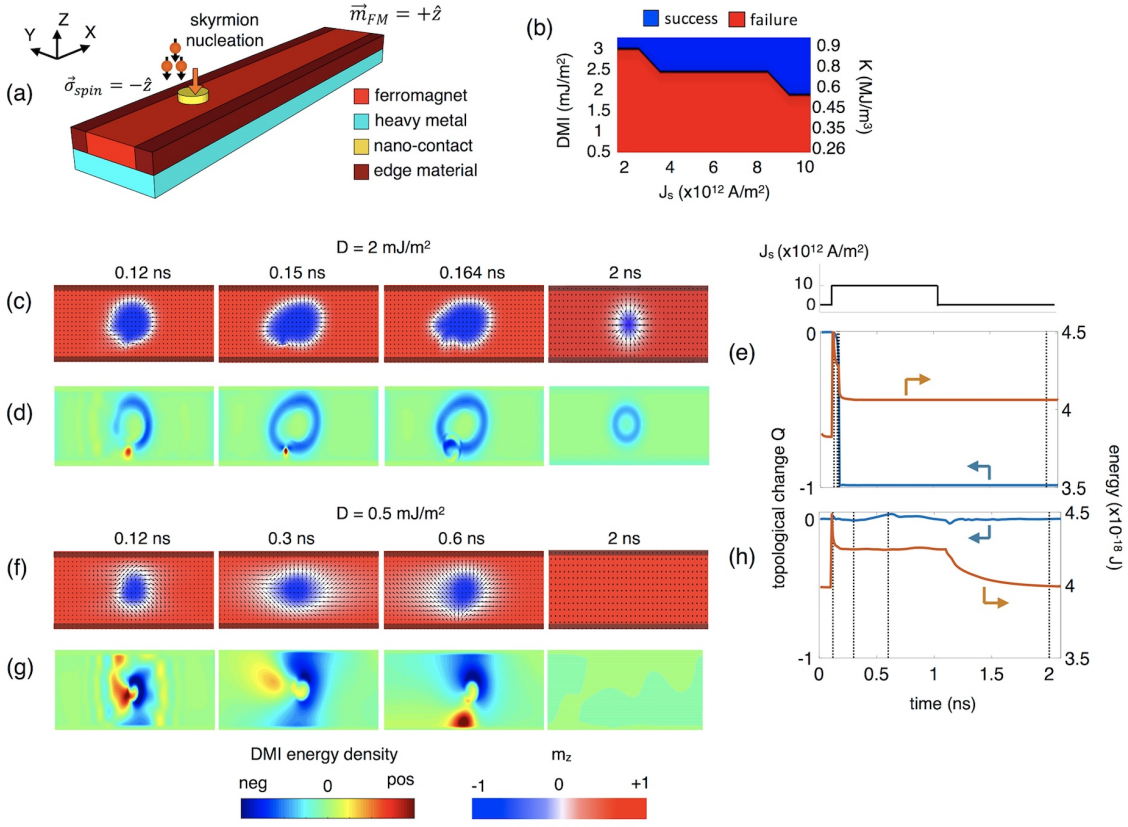

Figure 5.5: (a) Scheme of skyrmion nucleation in a nanowire with edge material exhibiting high PMA. (b) Probability of skyrmion nucleation in the presence of edge material for different values of (D, K) and injected spin current density J_s. (c, d) Temporal evolution of magnetization and corresponding DMI energy density after spin current injection for D = 2 mJ/m^2. (e) Change in the skyrmion number from 0 to -1 upon VBL annihilation and the change in the total energy. (f, g) Temporal evolution of magnetization and corresponding DMI energy density after spin current injection for D = 0.5 mJ/m^2. (h) Corresponding change in the skyrmion number and the total energy.

favored by DMI while shrinking the region with opposite chirality into the defect-like regions trapping a large positive DMI and exchange energy density as seen in Figure 5.5(d). At t = 0.16 ns, the size of this defect-like region decreases to a minimum, trapping a large amount of positive DMI energy density that forces the VBLs to get annihilated with rapid reorientation of the spins. As the VBL gets annihilated at t = 0.164 ns, the bubble relaxes to a skyrmion configuration with skyrmion number changing to a value close to -1 as seen in Figure 5.5(e) with a drastic reduction in the energy of the system.

However, for even lower DMI D = 0.5 mJ/m^2, we do not see an annihilation of the VBLs. On the contrary, the VBL pair exists throughout the duration of the applied spin current pulse as see in Figure 5.5(f). Additionally, we see that as the position of the VBLs change due the applied spin torque, the magnetic bubble relaxes, elongating in the longitudinal direction, as seen at t = 0.3 ns when the defect-like point aligns along the length of the nanowire. This also results in a decrease in the maximum positive DMI energy density concentrated at the defect-like regions of the pseudo-domain wall as seen in Figure 5.5(g). The positive DMI energy density attains its peak value when the defect-like point aligns along the transverse (y) direction as seen at t = 0.6 ns in Figure 5.5(f, g). However, this peak value of maximum positive DMI energy density remains unsuccessful in annihilating the VBLs. This points to the fact that there exists a threshold DMI strength or corresponding trapped positive DMI energy density that can force the spins inside the defect-like regions to reorient along the direction favored by DMI, thus annihilating the VBLs. As the current pulse stops after 1 ns, the magnetic bubble collapses to form the initial uniform ferromagnetic state. Figure 5.5(h) shows the change in the total energy and the skyrmion number.

Impact of Variation of Material Parameters

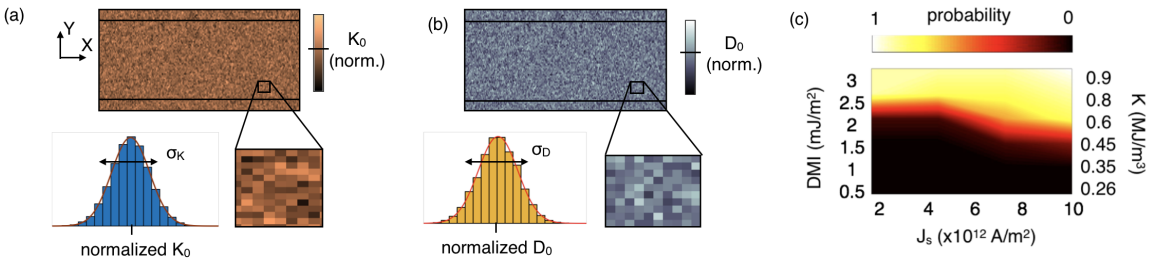

Figure 5.6: Scheme of a local site-by-site uncorrelated spatial variation of (a) PMA and (b) DMI used in the simulation. We use a normal distribution around a mean value of K_0 and D_0 with standard deviations (σ_K and σ_D) of 10%. (c) Probability distribution plot of nucleating a skyrmion in the presence of edge material for different values of (D, K) and injected spin current density J_s, which agrees well with the variation-free plot in Fig. 2(b) of the main text.

Since sputtered magnetic multilayers [240–242, 273] exhibit local variations of mag-

netic parameters which may lead to pinning and annihilation of VBLs, here we additionally study the impact of local variations in magnetic parameters which may lead to pinning and annihilation of VBLs using a local site-by-site uncorrelated variation of both PMA and DMI. We use a normal distribution around a mean value of K_0 and D_0 with a standard deviation (σ_K and σ_D) of 10% as shown in Figure 5.6(a) and (b). As shown in Figure 5.6(c), we do not see any significant variation in the result from that highlighted in Figure 5.5(b).

5.3.3 Skyrmion Nucleation in Nanowire with Gap in Edge Materia

Next, we investigate a novel mechanism of skyrmion nucleation via VBL expulsion by pinning the edge-to-edge domain wall using a narrow gap in the edge material. The proposed geometry is illustrated in Figure 5.7(a). The optimum choice of the gap length for successful skyrmion nucleation, as shown in Figure 5.7(b), is explained later. Figure 5.7(c) shows the skyrmion nucleation process with injected spin current density $J_S = 5 \times 10^{12}$ A/m^2 in the presence of D = 1 mJ/m^2 and a gap length of 20 nm. At t = 0.22 ns, the magnetization inside the nano-contact region is reversed forming the magnetic bubble containing the VBL pair. The position of the VBLs changes due the applied spin torque and as it aligns with the edge gap at t = 0.93 ns, the VBL gets attracted towards the edge initiating the formation of edge-to-edge domain wall. However, due to the presence of edge materials with high PMA on both sides of the gap, the edge domain wall gets pinned contrary to the case without edges as seen in Figure 5.4(h). The impact of the edge material with high PMA is similar to that of trapping a domain wall pair via pinning using notches or anti-notches [278, 279]. As the edge domain wall remains pinned forming a fractional edge skyrmion at t = 0.95 ns, the spins at the center of the gap where the net magnetization points in the z direction (blue region in Figure 5.7(c)) tilt outward due the boundary condition imposed by DMI [280]

$$\frac{d\vec{m}}{dn} = \frac{D}{2A}\left(\vec{z} \times \vec{n}\right) \times \vec{m} \tag{5.6}$$

where A is the exchange stiffness of the magnetic layer, $\vec{n}$ is the edge normal and $\vec{z}$ is the unit vector in the out-of-plane direction. This rapid reorientation of the spins in the gap regions along with the simultaneous pinning of the edge domain wall, prohibiting domain wall propagation, results in the re-generation of a magnetic bubble surrounded by a pseudo-domain wall but without any VBL (all spins pointing outward) as seen in zoomed-in picture of the gap region in Figure 5.7(d). Eventually, the bubble decouples from the edge-gap and moves towards the center of the nanowire due the repulsive force from the edges and relaxes into a stable skyrmion configuration accompanied by a change in the skyrmion number to a value close to -1 and reduction in the total energy as shown in Figure 5.7(e). As the spin current pulse stops after 1 ns, the skyrmion size shrinks to its intrinsic diameter and remains stable as seen at t = 2 ns. Thus, the proposed mechanism follows a pathway involving (a) creation of a magnetic domain with reversed magnetization surrounded by a pseudo-domain wall containing one or more pairs of vertical Bloch lines (VBLs), (b) formation of edge-to-edge domain wall as the VBL gets attracted towards the edge of the nanowire, (c) pinning of the edge-to-edge domain wall using notches or anti-notches as the VBLs get annihilated at the edge of the nanowire and (d) creation of magnetic bubble with defect-free domain wall eventually relaxing into a circular skyrmion structure. As highlighted in Figure 5.7(e), this mechanism allows sub-nanosecond skyrmion creation.

We further analyze the impact of the gap length in order to obtain an optimum range for successful skyrmion nucleation. We first consider the case of an extremely narrow gap length of 5 nm as shown in Figure 5.7(f). At t = 0.22 ns, the magnetic bubble forms and the position of the VBLs changes. However, as the VBL pair reaches the narrow gap at t = 0.9 - 0.92 ns, it moves past it without forming fractional edge skyrmion. This points to the fact that the minimum gap length must be at least equal to the domain wall width $\Delta_{DW} = \sqrt{A/K_{eff}}$ to support the two half domain walls (with the width of $\Delta_{DW}/2$ each) initiating the VBL annihilation process as shown in Figure 5.7(g). Figure 5.7(h) shows the change in the total energy and the skyrmion number remaining at 0. For the other

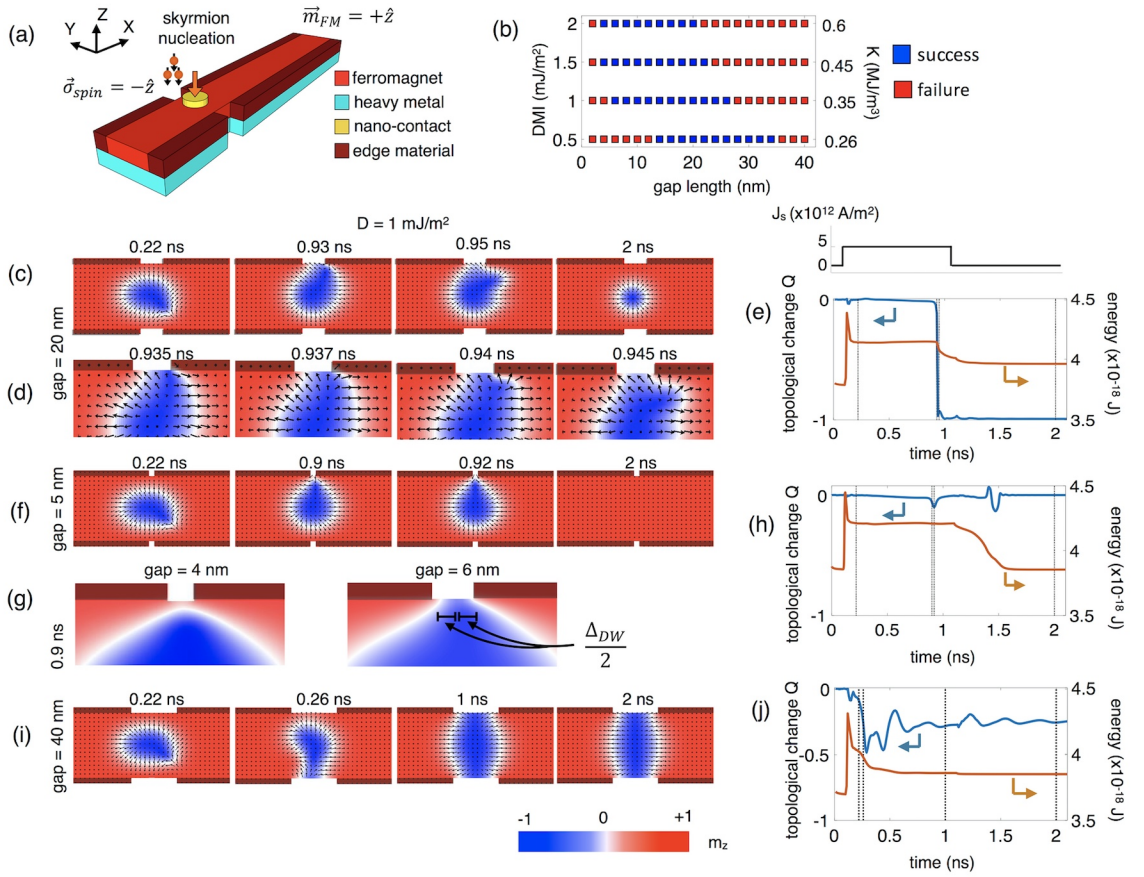

Figure 5.7: (a) Scheme of skyrmion nucleation using localized spin current injection into a nanowire with narrow gap in edge material. (b) Optimum gap length in the edge material for successful skyrmion nucleation for different values of D and K. (c) Temporal evolution of magnetization after spin current injection for D = 1 mJ/m^2. (d) Zoom-in of the gap region illustrating the skyrmion nucleation mechanism. (e) Change in the skyrmion number and the total energy for skyrmion nucleation process in the presence of a gap length of 20 nm. (f) Temporal evolution of magnetization in the presence of a narrow edge gap of length 5 nm showing an unsuccessful skyrmion nucleation. (g) Zoom-in of the gap region for two different gap lengths of 4 and 6 nm illustrating the requirement of a minimum gap length equal to the domain wall width $\Delta_{DW} = \sqrt{A/K_{eff}}$ for successful skyrmion nucleation. (h) Change in the skyrmion number and the total energy in the presence of a gap length of 5 nm. (i) Temporal evolution of magnetization in the presence of a wide edge gap of length 40 nm showing the formation of an edge-meron and finally a domain wall pair. (j) Change in the skyrmion number and total energy in the presence of a gap length of 40 nm.

extreme case of a wide gap, as shown in Figure 5.7(i) for a gap length of 40 nm, the VBL gets attracted towards the edge gap. On reaching the edge, the bubble transforms into an edge-meron or half skyrmion (with topological change Q = -1/2 as seen in Figure 5.7(j)) as

seen at t = 0.26 ns. The edge-meron either remains as an energetically meta-stable state or transforms into a pair of domain walls trapped between the anti-notches as seen at t = 1 ns. When the current pulse is turned off after 1 ns, the spin configuration collapses forming a uniformly magnetized nanowire as seen at t = 2 ns. Figure 5.7(j) shows the change in the total energy and the skyrmion number. The scenario when the edge-meron or domain wall pair becomes energetically more favorable than the skyrmion occurs when the gap length becomes greater than the size of the skyrmion, putting a limitation on the optimum gap length. Figure 5.7(b) shows the optimum gap length for successful skyrmion nucleation for different values of DMI and PMA. The upper and lower limits of optimum gap length obtained from micromagnetic simulations for all (D, K) pairs agree well with the above stated hypothesis. Similar results (not shown here) were obtained on reducing the spin current density to the threshold value of $J_S \geq 1.5 \times 10^{12}$ A/m^2.

5.3.4 Robustness to Variability

Recent experiments on the existence of room-temperature skyrmions in sputtered multilayers [240–242, 273] have observed the presence of local variations of magnetic parameters which leads to pinning and disordered motion of skyrmions. Since in ultra-thin films, local variations of thickness can dramatically change the thickness-dependent PMA and DMI, to incorporate such in-homogeneity, we use a local site-by-site uncorrelated variation of both PMA and DMI. Figure 5.8(a) and (b) show an example of spatial variation of PMA and DMI used in the simulation, respectively. We use a normal distribution around a mean value of K_0 and D_0 with a standard deviation (σ_K and σ_D) of 10% as shown in Figure 5.8(a) and (b). The probability distribution plot of nucleating a skyrmion for different values of DMI (and PMA) and gap length, highlighted in Figure 5.8(c), do not show any significant variation from Figure 5.7(b), thus illustrating the robustness of the nucleation process to 10% variability in PMA and DMI. To further elucidate the reliability of the nucleation mechanism, we calculate the probability of nucleation for simultaneous variation in PMA

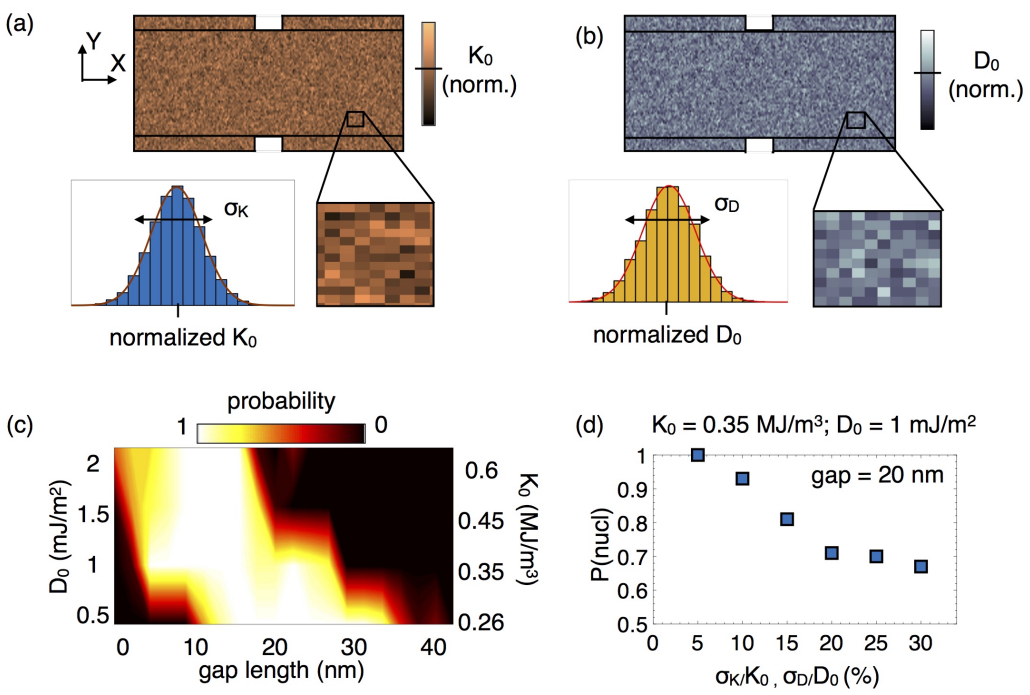

Figure 5.8: Scheme of a local site-by-site uncorrelated spatial variation of (a) PMA and (b) DMI used in the simulation. We use a normal distribution around a mean value of K_0 and D_0 with standard deviations (σ_K and σ_D) of 10%. (c) Probability distribution plot of nucleating a skyrmion for different values of DMI (and PMA) and gap length, which agrees well with the variation-free plot in Fig. 3(j) illustrating the robustness of the proposed nucleation mechanism. (d) Probability of nucleation for simultaneous variation in PMA and DMI (σ_K and σ_D) from 5-30% around the mean value of K_0 = 0.35 MJ/m^3 and D_0 = 1 mJ/m^2.

and DMI (σ_K and σ_D) up to 30% around the mean value of K_0 = 0.35 MJ/m^3 and D_0 = 1 mJ/m^2. As shown in Figure 5.8(d), the probability falls below 0.9 beyond a variation (σ_K and σ_D) of 10%. Also, note that we consider a pessimistic case of site-by-site variation in material parameter over a mesh size (comparable to grain size in crystalline film like Co) of 1 nm with no correlation in variation between the neighboring cells.

5.3.5 Skyrmion Nucleation in Nanowire with Notches as Pinning Sites

Having established that the edge material acts as pinning sites for edge domain wall and inspired by domain wall pinning at anti-notches, we next explore the possibility of skyrmion nucleation in a nanowire geometry in the presence of notches. The notches with dimensions 50 nm long and 5 nm wide are considered to be of the same material as the edges considered earlier (high PMA) that can act as pinning sites for the domain wall. Figure 5.9(a) illustrates the proposed structure consisting of 4 rectangular notches (pinning site). The optimum gap length for successful skyrmion nucleation for different values of DMI and PMA using notches is shown in Figure 5.9(b). Figure 5.9(c) shows the skyrmion nucleation process with injected spin current density $J_S = 5 \times 10^{12}$ A/m^2 in the presence of D = 1 mJ/m^2 and a gap length of 20 nm between the notches. The nucleation mechanism follows the same pathway as explained earlier with the formation of the magnetic bubble containing VBL as seen at t = 0.22 ns. At t = 0.63 ns, the VBL reaches the edge of the nanowire initiating the formation of the edge-domain wall. However, due to the presence of the notches at the edge of the nanowire, the domain wall gets pinned similar to Figure 5.7(c, d) forming a fractional edge skyrmion while the spins at the center of the gap reorient to point in the outward direction as dictated by the boundary condition imposed by DMI. At t = 0.65 ns, a magnetic bubble is re-generated surrounded by a pseudo-domain wall without any VBL. The bubble finally relaxes to a stable skyrmion structure. Figure 5.9(d) shows the zoomed-in picture of the gap regions showing the formation of the defect-free magnetic bubble. Figure 5.9(e) shows the change in the total energy and the skyrmion number highlighting sub-nanosecond skyrmion nucleation.

We further study the impact of the gap length between the notches or pinning sites on the skyrmion nucleation process. As shown in Figure 5.9(f), a narrow gap of 10 nm does not allow the formation of the edge domain wall, prohibiting the expulsion of the VBLs at the edge of the nanowire. Hence, the VBL pair moves past the gap without skyrmion nucleation. It is intriguing to find that the lower limit of gap length for successful skyrmion

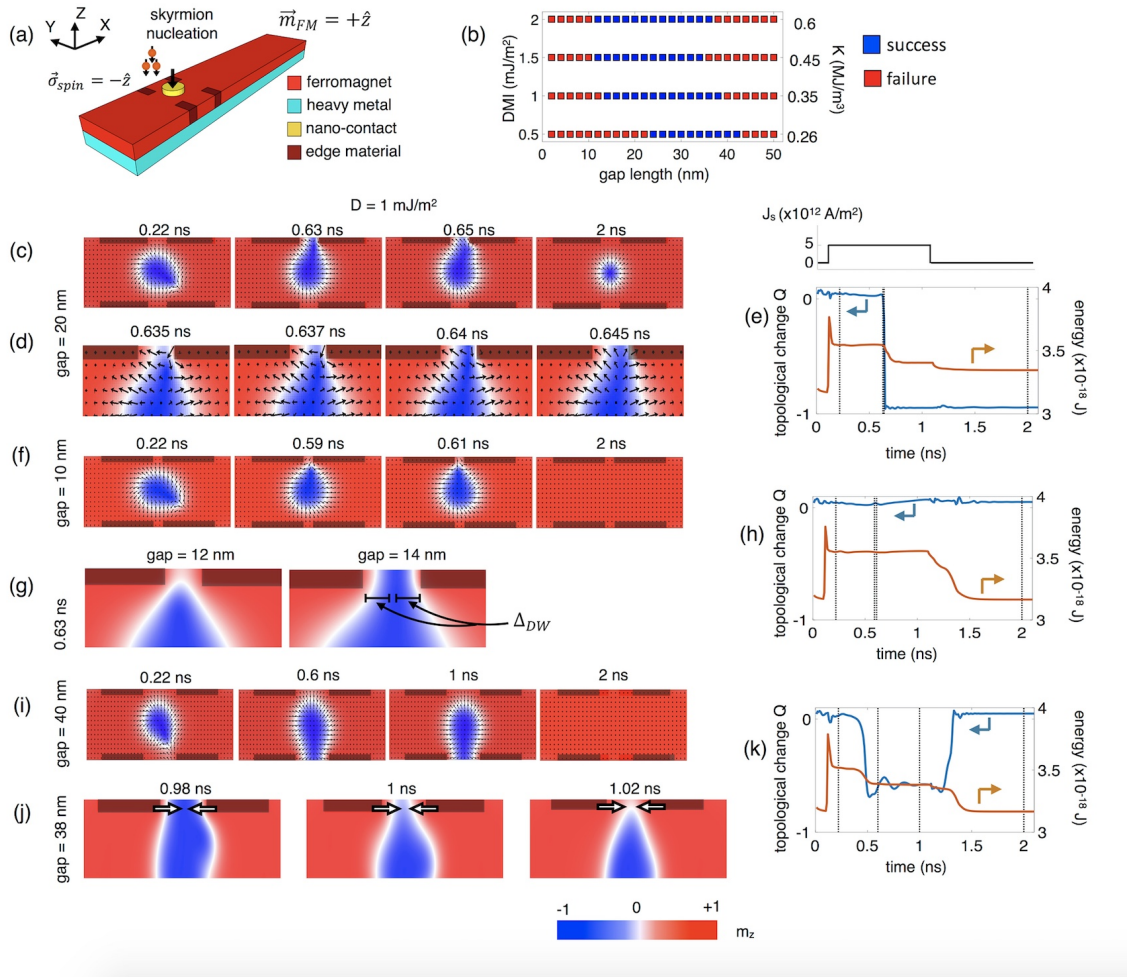

Figure 5.9: (a) Scheme of skyrmion nucleation in a nanowire with notches as pinning sites. (b) Optimum gap length between the notches for successful skyrmion nucleation for different values of DMI and K. (c) Temporal evolution of magnetization after spin-current injection for D = 1 mJ/m^2. (d) Zoom-in of the gap region between the notches illustrating the skyrmion nucleation mechanism. (e) Change in the skyrmion number and the total energy for skyrmion nucleation process in the presence of a gap length of 20 nm. (f) Temporal evolution of magnetization in the presence of a narrow gap of 10 nm between the notches showing an unsuccessful skyrmion nucleation. (g) Zoom-in of the gap region for two different gap lengths of 12 and 14 nm illustrating the requirement of a minimum gap length of $2\Delta_{DW}$ for successful skyrmion nucleation. (h) Change in the skyrmion number and the total energy in the presence of a gap length of 10 nm. (i) Temporal evolution of magnetization in the presence of a wide edge gap of length 40 nm showing the formation of an edge-meron. (j) Zoom-in of the gap region for a 38 nm gap length showing the additional repulsive force from the notches facilitating the generation of defect-free skyrmion bubble. (k) Change in the skyrmion number and the total energy in the presence of a gap length of 40 nm.

nucleation has increased to almost twice that of the previous case (see Figure 5.9(b)). As shown in Figure 5.9(g), the gap region between the notches or pinning sites now has to accommodate two domain wall widths Δ_{DW} for the VBL to reach the nanowire edge and get annihilated. Hence, the minimum gap length in this scenario increases to almost $2\Delta_{DW}$. Figure 5.9(h) shows the change in the total energy and the skyrmion number remaining at 0. For a wider gap, as shown in Figure 5.9(i), the bubble transforms into an edge-meron that becomes energetically more favorable than the skyrmion. The edge-meron exists as long as the current pulse remains on after which it gets annihilated at the edge of the nanowire. Figure 5.9(k) shows the change in the total energy and the skyrmion number Q changing to a value of -1/2 denoting the creation of an edge-meron for the duration of the applied current pulse. We also see an increase in the upper limit of the optimum gap length (see Figure 5.9(b)). This is due to an additional repulsive force applied by the notches or the pinning sites in the gap region on the two domain walls. As shown in Figure 5.9(j) for a gap of 38 nm, this additional repulsion forces the two domain walls to move towards each other resulting in the re-generation of the defect-free magnetic bubble as seen at t = 1.02 ns in Figure 5.9(j). The upper and lower limits of optimum gap length obtained from micromagnetic simulations for all (D, K) pairs as shown in Figure 5.9(b) agree well with the above stated hypothesis. Similar results (not shown here) are obtained on reducing the spin current density to the threshold value of $J_S \geq 1.5 \times 10^{12}$ A/m^2.

5.4 Spin-Orbit-Torque Driven Skyrmion Motion

Having established a nucleation mechanism for isolated skyrmions in a nanowire, next we investigate their current-induced motion along the nanowire. Recent theoretical and experimental investigations have revealed that skyrmions can be moved along a nanowire by in-plane spin-current injection (using spin-transfer-torque STT) or via vertical injection of spin current (using STT or spin-orbit-torque SOT). The microscopic phenomena of SOT have been discussed already in Section 3.4.2 and the Slonczewski-like SOT exerted can

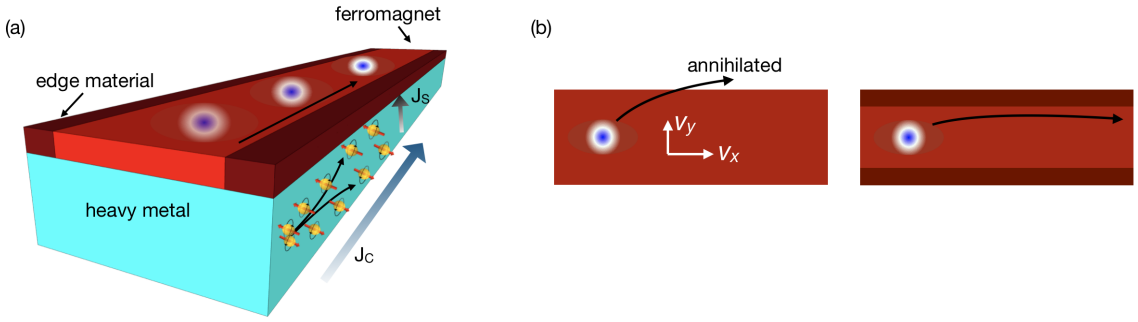

Figure 5.10: (a) Illustration of spin-orbit-torque driving skyrmions in a nanowire consisting of multilayers of heavy metal exhibiting high spin orbit coupling, ferromagnetic material and an oxide layer (MgO, not shown in the figure). (b) Schematic of overcoming skyrmion Hall effect and eventual annihilation at the edge of nanowire by using edge materials with high PMA.

be much stronger than STT from in-plane spin current. We mainly compare the spin Hall effect from platinum (Pt) and tantalum (Ta) for driving skyrmions due to their large spin Hall angle θ_{SHE}.

Figure 5.10(a) shows the schematic of driving skyrmions in a nanowire consisting of multilayers of heavy metal exhibiting high spin orbit coupling, ferromagnetic material and an oxide layer (not shown in the figure for simplicity). The material parameters used in simulation are listed in Table 5.1. Due to spin-orbit effect, the injected charge current J_C through the heavy metal generates a vertical spin current J_S that drives the skyrmion. The curent-driven skyrmion displays a longitudinal velocity v_x along x-direction and a transverse velocity v_y along y-direction due to skyrmion Hall effect. The transverse motion along y-direction stops at some distance from the edge of the nanowire due to the repulsive interaction from the tilted edge magnetization induced by DMI. However, increasing the driving current forces the skyrmion to reach the nanowire's edge and get annihilated, thus putting a limitation on the maximum current-induced velocity (see Figure 5.10(b, left). To avoid this scenerio, we again resort to the concept of incorporating an additional potential barrier at the two edges of the nanowire using a 5 nm wide edge material with high PMA, similar to that discussed in Section 5.3.2 (see Figure 5.10(b, right)).

5.4.1 Skyrmion dynamics from Thiele Equation

The current driven skyrmion dynamics can be well accounted by the Thiele equation

$$\vec{G} \times \vec{v} - \alpha D\vec{v} + F_{SHE} + F_C = 0 \tag{5.7}$$

where $\vec{G} = -4\pi Q\frac{\mu_0 M_S}{\gamma_o}t_{FM}\hat{z}$ is the gyrovector, D is the dissipative force tensor with elements $D_{xx} = D_{yy} = \frac{\mu_0 M_S}{\gamma_o}t_{FM}\left(\frac{\pi^3 R_{sky}}{\Delta_{DW}}\right)$ where R_{sky} is the radius of skyrmion, $\vec{v}$ is the skyrmion velocity, $F_{SHE} = \frac{\hbar\theta_{SHE}J}{2e}\pi^2\eta R_{sky}\hat{x}$ is the driving force due to spin Hall effect and $F_C \propto -f_0 e^{\frac{W-y}{R_{sky}}} + f_0 e^{\frac{W+y}{R_{sky}}} \approx -\kappa Y\hat{y}$ is the repulsive force from the nanowire edge or additional edge material introduced. Considering a pulse current (of pulse width t_P) applied to drive the skyrmion, the above equation can be analytically solved to provide the transient response

$$X(t < t_P) = \frac{F_{SHE}}{\alpha D}\left[t - \frac{G^2}{\alpha d\kappa}\left(1 - e^{-t/\tau}\right)\right] \tag{5.8}$$

$$X(t > t_P) = X(t_P) + \frac{G}{\alpha D}Y(t_P)\left[1 - e^{-(t-t_P)/\tau}\right] \tag{5.9}$$

$$Y(t < t_P) = \frac{GF_{SHE}}{\alpha D}\left(1 - e^{-t/\tau}\right) \tag{5.10}$$

$$Y(t > t_P) = Y(t_P)e^{-(t-t_P)/\tau}\Bigg] \tag{5.11}$$

with $\tau = \frac{G^2+\alpha^2 D^2}{\alpha D\kappa}$. This gives a transient longitudinal velocity of

$$v_x = \frac{F_{SHE}}{\alpha D}\left[1 - \frac{G^2}{G^2 + \alpha^2 D^2}e^{-t/\tau}\right] \tag{5.12}$$

with steady state velocity $v_{x,steady} \approx GF_{SHE}/\alpha D$. Figure 5.11(a) shows the longitudinal stead state velocity v_x as a function of the injected spin current density J_S for different values of DMI D and PMA K calculated from numerical simulations. The velocity shows a good linear dependence on the driving current density which agrees well with the above analytical expression. However, for a given J_S, the velocity decreases with reduction in

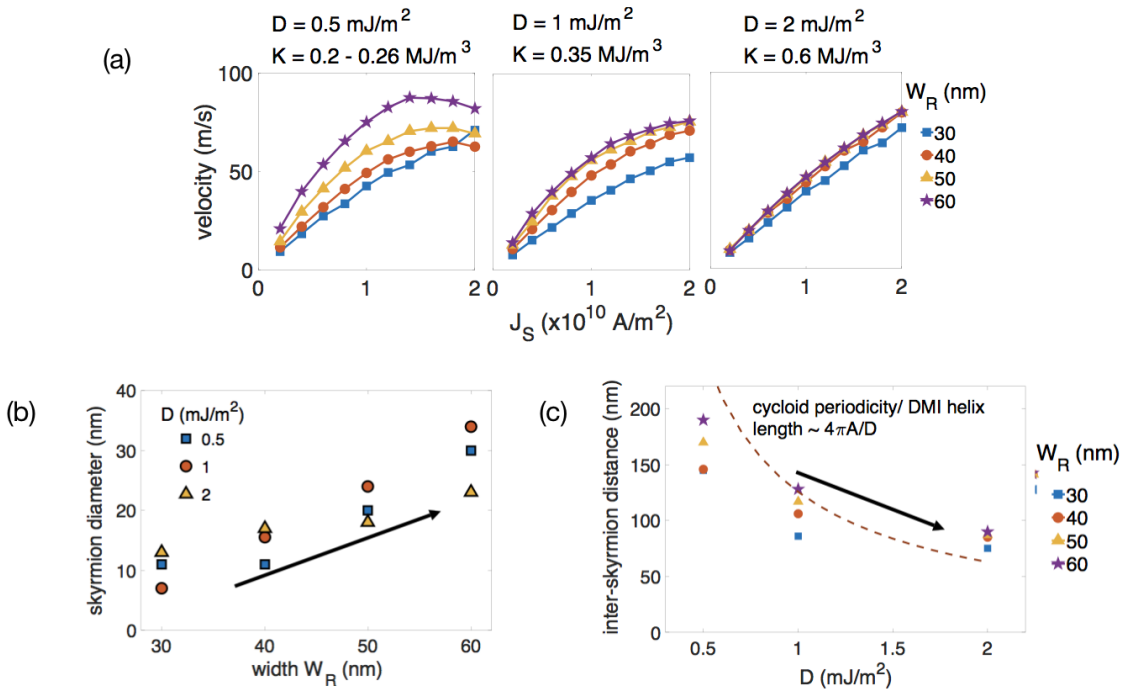

Figure 5.11: (a) Plot of velocity vs injected spin current density J_S for different values of DMI D and nanowire width W_R. (b) Plot of skyrmion diameter as a function of nanowire width W_R. (c) Plot of steady state spacing between the skyrmion in the nanowire as a function of the DMI D.

the width of nanowire W_R. This is because a narrower nanowire causes a highly confined skyrmion with a reduced skyrmion size as seen in Figure 5.11(b). As the velocity of the skyrmion directly depends on its size, a narrower nanowire leads to a reduction in the velocity.

5.5 Inter-Skyrmion Spacing

Another important parameter is the inter-skyrmion distance that ultimately dictates the throughput of the interconnect. The repulsive force between the skyrmions is given by [281]

$$F_{ss} = K_1\left(\frac{d\sqrt{H_K A}}{D}\right) \times \left(\frac{A}{t}\right) \tag{5.13}$$

where K_1 is the modified Bessel function and H_K is the perpendicular anisotropy field. The force F_{ss} drastically decreases when the spacing between the skyrmions increase. The inter-skyrmion distance can also be related to the helix length $L_D = 4\pi A/D$ which shows that increasing the DMI increases the tendency of the neighboring spins to curl or rotate and form closely packed skyrmions. For the purpose of studying the reliable and optimum skyrmion spacing in our simulations, we initially create two skyrmions in the nanowire at a specific distance and then allow the configuration to relax. Due to the repulsive force F_{ss} between the skyrmions, the spacing between them as well as their sizes will change with time. We record the steady state distance between them as a function of the DMI D and nanowire width W_R as seen in Figure 5.11(c). We see a stronger dependence on the DMI rather than on the wire width. The width primarily dictates the skyrmion size (see Figure 5.11(b)), hence a smaller width stabilizes smaller skyrmions that can be packed more closely as seen in Figure 5.11(c).

5.6 Skyrmion Detection

A key challenge of skyrmion based logic, memory and interconnect is to electrically detect individual skyrmions. Several techniques have so far been proposed utilizing magnetic tunnel junction (MTJ), non-collinear magneto-resistance (NCMR) [282] and utilizing the topological Hall effect [283]. However, for skyrmion interconnect connecting magnetic logic, one can also envision a direct conversion of skyrmion to a stable magnetic configuration that can again be utilized by the magnetic logic blocks. This, however, lies beyond the scope of the present research and has been discussed briefly in the future works.

5.7 Performance Analysis of Skyrmion Interconenct

We conclude this chapter by evaluating the performance of skyrmion interconnect and comparing it with other proposals for spintronic interconnect. We consider two representative cases based on the choice of materials

- Ta/CoFeB with an experimentally observed feasible DMI of 0.5 mJ/m^2.
- Pt/CoFeB with an experimentally observed feasible DMI of 1 mJ/m^2.

The energy dissipation associated with moving a single skyrmion along the length of the interconnect is given by

$$E = \frac{J_S^2}{\left[\theta_{SHE}\left(1 - sech(t/\lambda_{s,HM})\right)\right]} \rho_{HM} t_{HM} W_R L \times \tau_{int} \tag{5.14}$$

where ρ_{HM} is the resistivity of the heavy metal, L and W_R are the length and width of the nanowire. The delay associated with moving a single skyrmion along the length of the interconnect is given by $\tau_{int} = L/v_x$. However, skyrmions can be packed closely together in a nanowire with spacing $\sim$ 100 nm or less (depending of the choice of material). Hence, the important metrics to focus on would be the throughput (or bit rate), energy/bit and bandwidth density. Throughput is calculated as v_x/S where S is the inter-skyrmion distance, energy/bit calculated as power/throughput and bandwidth density measured by bit rate per unit width.

Figure 5.12(a) shows the energy/bit as function of interconnect length for the two representative skyrmion interconnects and comparison with various other spintronic interconnects. Platinum (Pt) proves to be a better option over Tantalum (Ta) owing to its lower resistivity. The value of DMI has little impact. The figure also shows a comparison with various other candidates for spintronic interconnect. All-spin logic (ASL) and conventional spin valve (CSV) interconnects utilize particle-based spin drift-diffusion mechanism for transmission of information. CSV proves to be more energy-efficient compared to ASL due to the absence of shunt path. Metallic interconnects like Cu and Al consume less power in the short interconnect regime due to their lower resistivities; however, in the intermediate regime (over 1 μm), the energy dissipation in metallic channel increases rapidly because of short spin relaxation lengths [259]. Semiconductor channel like Si provides a better option

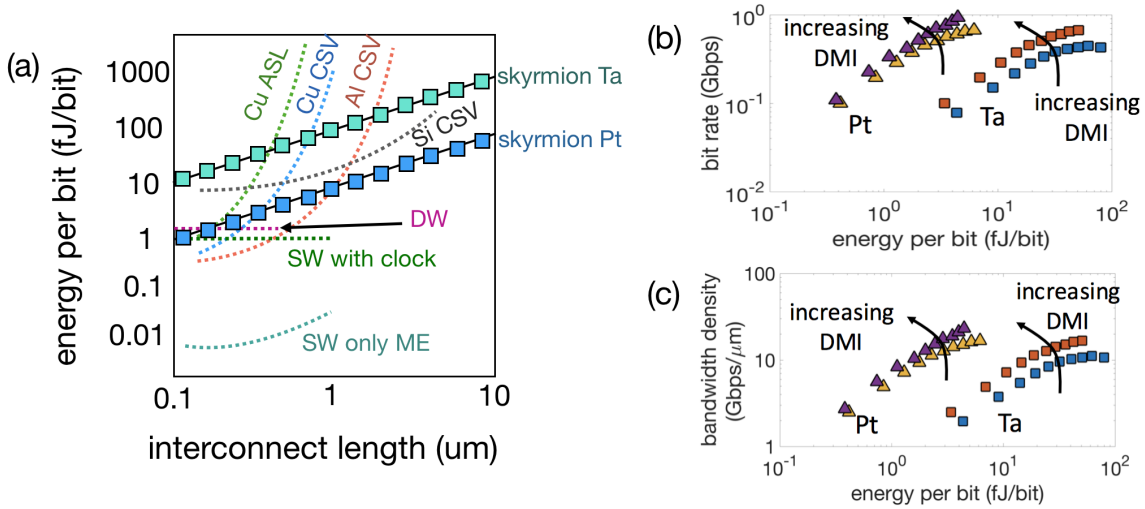

Figure 5.12: (a) Comparison of energy/bit for various spintronic interconnects as a function of interconnect length, (b) Plot of bitrate vs. energy/bit calculated for a skyrmion interconnect of length 1 μm and (c) Plot of bandwidth density vs. energy/bit calculated for a skyrmion interconnect of length 1 μm.

over metallic channel for longer interconnects since it has longer spin relaxation time and its spin relaxation length can be improved by applying an electric field [258]. However, as seen in Figure 5.12(a), skyrmion interconnect dissipate lower energy/bit compared to spin drift-diffusion interconnects in the intermediate regime (over 1 μm). A recent proposal by Chang et al. [260] introduced the concept of automotion of domain wall for connecting ASL. However, it proved to be effective only for short interconnects ($\sim$ 400-500 nm) since the domain wall stops moving due to the dissipative damping process. It is anticipated that current driven domain wall will dissipate energy/bit in the same range as skyrmion interconnect. However, domain walls are more prone to getting pinned at defects than skyrmions; hence, skyrmion interconnect would be more robust than domain wall interconnect in the intermediate regime. As seen in Figure 5.12(a), spin wave provides an energy-efficient alternative, even after including the energy dissipation in the clocking circuit. However, as has been highlighted earlier, it requires clocking at regular intervals for signal amplification and non-reciprocity. Such a requirement is absent for skyrmion interconnect. Note that the energy/bit for skyrmion interconnect in Figure 5.12(a) only includes the energy

dissipated during the transport of skyrmions. Assuming a nucleating spin current density $J_S \sim 1.5 \times 10^{12} A/m^2$ injected through a CSV and nano-contact of diameter around 20 nm, we estimate the net charge current to be in the range of 0.3 0.5 mA and an additional energy dissipation for skyrmion nucleation in the range of 2 - 5 fJ.

Figure 5.12(b) shows the plot of throughtput (or bit rate) as a function of energy/bit for a 1μm long skyrmion interconnect. As mentioned earlier, Pt offers lower energy/bit due its lower resistivity. Additionally, a higher DMI value lowers the spacing between skyrmions, thus increasing the throughput and lowering the energy/bit. For achieving the same throughput, transport via spin drift-diffusion mechanism would dissipate higher energy compared to skyrmion interconnect. Finally, we also plot the bandwidth density vs energy/bit for a 1μm long skyrmion interconnect as seen in Figure 5.12(c) which follows a similar trend as shown in Figure 5.12(b).

CHAPTER 6
CONCLUSION AND FUTURE DIRECTIONS

After more than four decades of exponential growth resulting in around 8 orders of magnitude improvement in the performance of electronic integrated circuits, it is now apparent that improving the energy efficiency of computing is going to be a major challenge. Therefore, there is a global search for information processing elements that use computational state variables other than electronic charge. Such devices are being sought after to bring in new functionalities and to further lower the power dissipation in computers. These new information processing devices, called the "Beyond-CMOS" technologies, encode information using various physical quantities which we call the "computational variables" or "state variables". While charge-based devices rely on the presence or absence of charge for denoting logic "1" and "0", respectively, non-charge based alternatives aim at utilizing various other physical quantities like electric dipole, spin, orbital state and light intensity, and often collective states. Two of them - electron spin and plasma oscillation have been the subject of discussion in this thesis. Most importantly, we focus on collective excitations like magnons, skyrmions and plamsons that provide new opportunities and attractive features like non-volatility, low-power computing and high-throughput. The work can be broadly divided into two categories - emerging logic and emerging interconnect.

6.1 Contribution of this Research

6.1.1 Magnonic Logic

Spin waves are propagating disturbances in magnetically ordered materials, analogous to lattice waves in solid systems and are often described from a quasiparticle point of view as magnons. The attractive advantages of Joule-heat-free transmission of information, utiliza-

tion of the phase of the wave as an additional degree of freedom and lower footprint area compared to conventional charge-based devices have made spin waves or magnon spintronics a promising candidate for beyond-CMOS wave-based computation. The possibility of using spin waves for information transmission and processing have been discussed. We have theoretically demonstrated the possibility of building a complete spin wave logic device. The integration of the magnetoelectric (ME) cells with the spin wave bus (SWB) provides a possible route for low power excitation and detection of spin waves and for non-volatile memory element. We identified suitable materials for the ME cell and PMA SWB using experimentally demonstrated parameters. The chosen materials for the SWB and ME cell are appealing owing to their ability to sustain a propagating spin wave via low damping and reduced PMA, high product of coupling coefficient to enable ultra-low power dissipation, ease of fabrication and material compatibility. We provide a pipelining scheme by introducing a multi-phase clocking scheme. The clocking scheme takes care of non-reciprocity (uni-direction signal flow) and sequential transmission of information. The re-generation of spin waves at each stage provides an automatic amplification to take care of the propagation loss. Thermal reliability is an important aspect that must be taken into consideration for spintronic devices. We explored the impact of thermal noise on the magnetization dynamics of the ME cell and in terms of the phase noise of the spin waves. A salient feature of this work is to enable thermally reliable phase-dependent switching of the spin wave detector. We identified a novel route of changing the energy landscape and utilizing a "saddle-point based" magnetization switching.

So far, the key focus has been to design an efficient nonvolatile spin-wave logic device. However, a key aspect of designing the spin-wave bus network is to ensure a low crosstalk noise level for guaranteeing signal integrity. The crosstalk being a strong function of the spacing between the lines can become an issue as the lines get closer due to routing or near the points where the spin-wave buses merge in a logic circuit like a majority gate, and thus putting a limitation on the design, routing, and placement of spin-wave bus net-

work. We investigated the crosstalk coupling between two adjacent co-planar spin-wave interconnects using rigorous numerical micromagnetics, and derived a compact physical model using analytical expressions, which demonstrates a good match with the actual full micromagnetic simulation results. Further, the work enabled the realization of two primary logic gates - inverters and majority gates, that lie at the heart of wave-based computing and together with the new emerging novel logic synthesis technique can open up and enable the true potential of the field of spin waves. Any novel technology must be complimented by a fast and energy-efficient transducer technology for signal conversion between the charge and spin domain. We proposed a comprehensive scheme for building spintronics transducers for back and forth signal conversion between spin and charge domains in addition to the associated CMOS peripheral circuitry. We performed systematic analysis of the impact of the transducers on the performance of SWD in terms of energy and area overhead. Performance evaluation of SWD compared with 7nm FinFET CMOS technology at the circuit level, yields a $3\times$ smaller area and up to an order of magnitude ($\sim 10\times$) lower energy-delay product (EDP) for large complex circuits with low overhead. Overall, SWD may outperform CMOS with increasing ratio of (logic size/overhead).

6.1.2 Plasmonic Logic

Alternative to electron spin, the oscillation of free electron density called "plasmons" provide an exciting new opportunity towards building nano-scale devices at the size of electronics but with the speed of photonics. Drawing analogies from the spin wave counterpart, we utilize the surface-plasmon-polariton (SPP) waves propagating at the interface between a metal and a dielectric to perform wave-based computing. Contrary to the state-of-the-art plasmonic logic devices, we use the phase of the wave instead of the intensity as the state or computational variable. We proposed and demonstrated a comprehensive scheme for building a nanoscale cascadable plasmonic inverter gate and majority logic gate along with a novel referencing scheme that can directly translate the information encoded in the

amplitude and phase of the wave into electric field intensity at the output. These primitive logic gates can further enable the efficient realization of complex logic gates like adders and multipliers.The proposed device demonstrates non-Boolean computational capability and the extremely high throughput enables direct usage in high throughput low latency signal processing applications which are arithmetic-heavy with strict timing requirements, like a pattern recognition system.

6.1.3 Skyrmion Interconnect

Any novel logic device technology must be complemented by a fast and energy efficient interconnect technology. Recently, magnetic skyrmions have been the focus of intense research with promising applications in memory, logic and interconnect technology. Relying on the small size, high-packing density, displacement via ultra-low current density, and robustness to defects and pinning, a skyrmion-based magnetic interconnect can provide a low-power, high throughput and robust alternative to other candidates for interconnecting magnetic logic without using a transduction for charge to spin signal conversion. A key ingredient for any skyrmion-based memory, logic or interconnect is an efficient, reliable and controlled scheme of nucleation or writing of magnetic skyrmions with reduced complexity. We propose a novel scheme for a controlled single skyrmion nucleation in a confined nanowire geometry with sub-100 nm width using a generalized approach of localized spin current injection technique in material systems exhibiting low DzyaloshinskiiMoriya interaction (DMI). Using spin-orbit-torque induced motion of skyrmions, we study the dependence of skyrmion velocity on the injected spin current density. Our study revealed that skyrmions can offer sub-100 nm spacing between them giving rise to high packing density. The performance of skyrmion interconnect in terms of energy-delay, energy/bit, bit-rate and bandwidth density has also been discussed and compared to other spintronic interconnects.

6.2 Impact on Other Related Research

The notion of using magnetoelectric (ME) effect, specifically magnetostriction, for "saddle-point" based switching introduced in this work also spurred active research for building other ME-assisted spintronic devices. A recently proposed ME-assisted spin-transfer-torque switching of magnetization resulted in an order of magnitude smaller pulse pulse width down to pico-seconds. Incorporating this in all-spin logic resulted in a 45× and 81× improvement in delay and energy for a 32-bit adder (more than 1000× improvement in EDP) [262].

The developed SPICE circuit model for spin wave bus is limited to 1-D micromagnetics. Such a model ignores any spatial variation of magnetization along the width or thickness of the magnetic film. Utilizing the micromagnetics-based SPICE model developed in this research, ongoing efforts are being made to extend the model to 2-D or even 3-D that will be capable of studying domain wall or skyrmion dynamics.

6.3 Future Work

6.3.1 Wave-Pipelining for Non-Volatile Magnonic Logic

A future step towards magnonic logic would be to to utilize the thermally reliable non-volatile magnonic logic device developed in this research with the wave-pipelining algorithm developed by Odysseas et. al. [66]. Accounting for the overhead provided by buffer-insertion to equalize all data path and restricting fan-outs will provide more accurate results in terms of performance analysis and comparison with CMOS.

6.3.2 Phase-Field Modeling of Ferroelectrics

Building on top of the work presented in this thesis on magnetoelectric (ME) effect, a future step would be to implement a phase-field modeling of the ferroelectric material. Analytical thermodynamics provides an alternative approach, but typically assume homo-

geneous single-domain ferroelectric phase with static switching processes, i.e., uniform time-independent applied electric field. However, ferroelectric thin films generally contain domain structures where the polarization and strain are in-homogeneous, and the total free energy is a function of all the spatially dependent order parameters. Additionally, the phenomena of electric-field-induced strain in a ferroelectric/ferromagnetic heterostructure can cause spatially varying strain due to ferroelastic domain nucleation, wall motion and mechanical relaxation. To capture the dynamic evolution of ferroelectric domains under an applied electric-field and study the effect of non-uniform strain on magnetization, a phase-field modeling approach needs to be employed. Analogous to the micromagnetic modeling approach, phase-field modeling involves investigating the kinetic evolution of spatial distribution of local polarization vector $P(x)$ described by the time-dependent Ginzburg-Landau (TDGL) equation.

6.3.3 Fully-Coupled Magnetic-Logic Skyrmion-Interconnect Model

Skyrmion-based interconnect have been introduced as a promising interconnect opportunity for interconnecting magnetic logic. We have proposed a nucleation mechanism via localized spin current injection. A future work in this direction would be to develop a comprehensive model by integrating a magnetic logic with the skyrmion interconnect. This would involve nucleation of magnetic skyrmions in a nanowire directly from a magnetic logic (like all-spin-logic or domain wall logic) and direct conversion of skyrmions to stable magnetic orientation for magnetic logic (all-spin-logic or domain wall logic). Spin-circuit models for all-spin-logic or domain wall logic can be integrated with micromagnetic simulations or compact models for skyrmion dynamics.

6.3.4 Developing Skyrmion Read-Out Mechanism

Several techniques have so far been proposed for detecting skyrmions like utilizing magnetic tunnel junction (MTJ), non-collinear magneto-resistance (NCMR) [282] and utilizing

the topological Hall effect [283]. A current-perpendicular-to-plane (CPP) provides an attractive option that can be achieved in an MTJ structure. However, this requires a rigorous calculation of the tunneling spin-mixing magnetoresistance and can be the focus of future work.

Appendices

APPENDIX A

CALCULATION OF PERPENDICULAR MAGNETIC ANISOTROPY (PMA) OF SPIN WAVE BUS

The origin of magnetic anisotropy can be attributed to two mechanisms: (a) the long range magnetic dipolar interaction which gives rise to the shape anisotropy, and (b) the spin-orbit interaction which gives rise to magnetocrystalline anisotorpy and magnetoelastic anisotropy. The perpendicular magnetic anisotropy (PMA) arises from this spin-orbit interaction at the interface which has a lowered symmetry; hence, behaves differently from bulk magnetic anisotropy. Specifically, theoritical prediction by Daalderop et. al. [103] in Co/Ni multilayer system has revealed the PMA to be arising from the spin-orbit interaction of states with $d_{x^2-y^2}$ and d_{xy} character present close to the Fermi level.

Phenomenologically, the total effective magnetic anisotropy can be separated into a volume contribution K_V and a surface contribution K_S and can be expressed as a function of the Co and Ni layer thicknesses t_{Co} and t_{Ni} and number of bilayer repetitions n as [101–105]:

$$K^{eff}D = K_V^{Co}t_{Co} + K_V^{Ni}t_{Ni} + 2K_S^{Co/Ni} + \frac{1}{n}\left[K_S^{Co/Pt} + K_S^{Ni/Cap} - K_S^{Co/Ni}\right] \quad \text{(A.1)}$$

where D is the bilayer thickness ($D = t_{Co}+t_{Ni} = (1+\alpha)t_{Co}$), $\alpha = t_{Ni}/t_{Co}$ is the thickness ratio and K_V^{Co} and K_V^{Ni} are the volume anisotropies of Co and Ni layers, respectively. $K_S^{Co/Ni}$, $K_S^{Co/Pt}$ and $K_S^{Co/Cap}$ are the interface anisotropies of Co/Ni, bottom Co/Pt and top Ni/Cap interfaces, respectively, considering the deposition of the Co/Ni multilayer on an underlayer of Pt and capped with a top capping layer, say Ta. Neglecting the effect of top cap layer, and assuming the following parameters: K_V^{Co}=-1 MJ/m^3, K_V^{Ni}=-0.12 MJ/m^3, $K_S^{Co/Ni}$=0.22 mJ/m^2, $K_S^{Co/Pt}$=0.88 mJ/m^2, we calculate the PMA of the multilayer as a

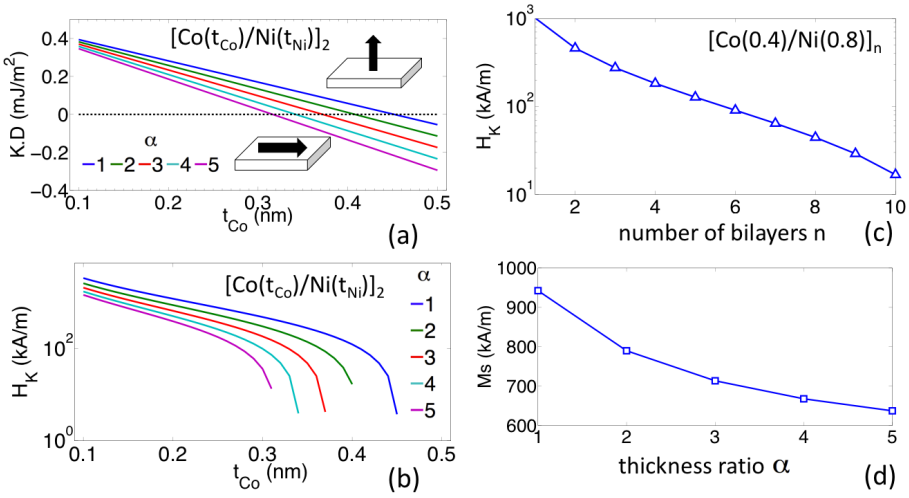

Figure A.1: (a) Variation of K.D as function of the thickness of the Co layer t_{Co} in the Co/Ni multilayer stack. A positive value indicates a PMA case while negative indicates in-plane magnetization. (b),(c) Variation of the anisotropy field H_K with the thickness of the Co layer t_{Co} and the number of bilayers n. (d) Variation of saturation magnetization of multilayer stack with the thickness ratio α.

function of the Co layer thickness t_{Co} for a fixed number of bilayers n = 10 as shown in Figure A.1(a,b) and as a function of n for a fixed thickness ratio α of 2 as shown in Figure A.1(c).

The effective saturation magnetization of the multilayer is calculated as

$$M_S = \left(M_S^{Co} t_{Co} + M_S^{Ni}\right)/D \tag{A.2}$$

where M_S^{Co} and M_S^{Ni} are the saturation magnetization of the Co and Ni layers with assumed valued of 1.4 MA/m and 485 kA/m, respectively. Figure A.1(d) the calculated effective M_S as function of the thickness ratio α.

APPENDIX B

GREEN'S FUNCTION APPROACH TO SPIN WAVE DISPERSION CALCULATION

Let us consider a rectangular ferromagnet as shown in Figure B.1. The external magnetic field H is applied in the z direction to saturate the magnetization M_S of the film parallel to the applied field except at the edges where edge domains may form.

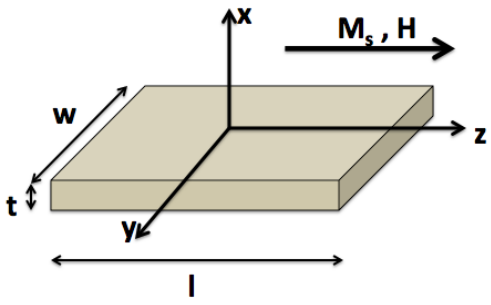

Figure B.1: Schematic of the ferromagnetic film. The external magnetic field H is applied in the z direction and M_s is parallel to the applied field.

Since we are interested in the linear oscillations of the magnetization, we assume the variation in the component of the magnetization in the z-direction, i.e., along the direction of the applied field to be much smaller than the transverse components, i.e. $m_z << m_x, m_y$; hence, the magnetization vector can be represented as:

$$\vec{M}(\vec{r}) = m_x(\vec{r})\hat{x} + m_y(\vec{r})\hat{y} + M_s\hat{z} \tag{B.1}$$

where $\vec{r} = x\hat{x} + y\hat{y} + z\hat{z} = x\hat{x} + \vec{\rho}$. We further assume the ferromagnetic film to be thin so that the distribution of magnetization in $\hat{x}$ is considered uniform. Thus $\vec{M}(\vec{r}) = \vec{M}(\vec{\rho})$.

We now resort to the theory developed by Kalinikos and Slavin [72] for the dispersion characteristic of spin waves in ferromagnet taking into account both the dipole-dipole in-

teraction and the exchange coupling. We use the tensorial Green's function formalism. In this formalism, the linearized Landau-Lifshitz equation of motion and Maxwell equations in the magnetostatic limit are reduced to an integro-differential equation for magnetization vector amplitude $\vec{m}(\rho) = m_x(\vec{\rho})\hat{x} + m_y(\vec{\rho})\hat{y}$ of the dynamic variable magnetization $\vec{m}(\vec{\rho}, t) = \vec{m}(\vec{\rho})exp(i\omega t)$,

$$\Big[-\alpha\omega_M \vec{\nabla}_\rho^2 + \omega_{H_i}(\vec{\rho})\Big]\hat{\mathbf{I}} \cdot \mathbf{m}(\vec{\rho}) + i\omega\hat{\mathbf{T}} \cdot \mathbf{m}(\vec{\rho}) - \omega_M \int d\rho' \hat{\mathbf{G}}_{x,y}(\vec{\rho}, \vec{\rho}')\mathbf{m}(\vec{\rho}) = 0$$

where

$$\hat{\mathbf{I}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}; \quad \hat{\mathbf{T}} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}; \quad \hat{\mathbf{G}}_{x,y} = \begin{bmatrix} G_{x,x} & G_{x,y} \\ G_{y,x} & G_{y,y} \end{bmatrix}; \quad \mathbf{m} = \begin{bmatrix} m_x \\ m_y \end{bmatrix} \tag{B.2}$$

and $\omega_M = \gamma 4\pi M_s$, $\alpha = A/2\pi M_s^2$ is the exchange constant and $\vec{\nabla}^2 = \partial^2/\partial y^2 + \partial^2/\partial z^2$,

$$\omega_{H_i} = \gamma H_i(\vec{\rho}); \quad H_i(\vec{\rho}) = H - N_{z,z}(\vec{\rho}).4\pi M_s; \quad N_{z,z}(\vec{\rho}) = -\int d\vec{\rho}' G_{z,z}(\vec{\rho}, \vec{\rho}') \tag{B.3}$$

where $N_{z,z}$ is the coordinate dependent demagnetizing factor for a rectangular prism. The first term in the integro-differential equation represents the exchange interaction, the second term denotes the static demagnetizing field, the term with ω arises from the time derivative of the LL equation and the last term represents the dynamic demagnetization in the film. Although the integro-differential equation can be solved numerically, it is fairly complicated and hence an approximate analytical expression for the dispersion relation is coveted.

B.1 Approximate Analytical Technique

The main assumption in this approach is the film is thin so that $t \ll L$ and $t \ll w$. It is known that the dipole-dipole matrix element depends on these aspect ratios and hence are also small. Considering such an approximation, the exact form of the dipole-dipole matrix

is not important, and we can use an approximate expression for the dipole-exchange spin wave dispersion as formulated by Kalinikos and Slavin [72]. The approximate dispersion equation representing the discrete frequencies of the spin wave eigenmodes of a rectangular magnetic film is given by:

$$\omega_{mn}^2 = \left(\omega_H^{mn} + \alpha\omega_M\kappa_{mn}^2\right)\left[\omega_H^{mn} + \alpha\omega_M\kappa_{mn}^2 + \omega_M F_{mn}(\kappa_{mn}L)\right] \tag{B.4}$$

where ω_H^{mn} represents the effective internal field given by the effective demagnetization factor N_{nm} as

$$\omega_H^{mn} = \omega_H - \omega_M N_{nm} \tag{B.5}$$

$$N_{nm} = \frac{4}{wl}\int d\vec{\rho} m_{mn}^2(\vec{\rho}) N_{zz}(\vec{\rho}) \tag{B.6}$$

$F_{mn}(\kappa_{mn}L)$ plays the role of a quantized matrix of the dipole-dipole interaction:

$$\begin{aligned} F_{mn}(\kappa_{mn}L) &= 1 + P(\kappa_{mn}L)\Big[1 - P(\kappa_{mn}L)\Big]\left(\frac{\omega_M}{\omega_H^{mn} + \alpha\omega_M\kappa_{mn}^2}\right)\left(\frac{\kappa_{my}^2}{\kappa_{mn}^2}\right) \\ &\quad -P(\kappa_{mn}L)\left(\frac{\kappa_{nz}^2}{\kappa_{mn}^2}\right) \end{aligned} \tag{B.7}$$

with

$$P(\kappa_{mn}L) = \left(1 - \frac{1 - e^{-qL}}{qL}\right); \quad \kappa_{mn}^2 = \kappa_{my}^2 + \kappa_{nz}^2 \tag{B.8}$$

APPENDIX C

DISPERSION RELATION OF SURFACE PLASMON POLARITON WAVE

The plasmon was initially described by David Pines and David Bohm in 1952 using the long-range electron-electron correlations [170]. Since plasmons are the quanta of a classical plasma oscillations, they can be described using the well-known Maxwell's equations

$$\vec{\nabla} \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}; \quad \vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}, \qquad \vec{\nabla} \cdot \vec{B} = 0; \quad \vec{\nabla} \cdot \vec{D} = \rho \tag{C.1}$$

In the absence of external charge and current densities, one can derive the well-known electromagnetic wave theory

$$\nabla^2 \vec{E} - \frac{\epsilon}{c^2} \frac{\partial^2 \vec{E}}{\partial t^2} = 0 \tag{C.2}$$

Assuming a harmonic time-domain electric field $\vec{E}(\vec{r}, t) = \vec{E}(\vec{r})e^{-i\omega t}$, one gets the Helmholtz equation for propagating wave

$$\nabla^2 \vec{E} + k_0^2 \epsilon \vec{E} = 0 \tag{C.3}$$

where $k = \omega/c$ is the wave vector of the propagating wave in vacuum.

A simplified geometry is assumed where the waves propagate along the x-direction and has no spatial variation along y-direction. Also, ϵ depends on one coordinate (z). The propagating wave can then be described as $\vec{E}(x, y, z) = \vec{E}(z)e^{i\beta x}$ where β is the complex propagation constant. The Helmholtz equation results in

$$\frac{\partial^2 \vec{E}}{\partial t^2} + (k_o^2 \epsilon - \beta^2)\vec{E} = 0 \tag{C.4}$$

Eqn. C.4 is the starting point for any analysis of guided electromagnetic mode in a waveguide. For a harmonic time-dependent wave propagating in the x-direction and homogeneity

along y-direction, a system of equations is obtained

$$\frac{\partial E_y}{\partial z} = -i\omega\mu_0 H_x; \quad \frac{\partial E_x}{\partial z} - i\beta E_z = i\omega\mu_0 H_y; \quad i\beta E_y = i\omega\mu_0 Hz \tag{C.5}$$

$$\frac{\partial H_y}{\partial z} = -i\omega\epsilon_0\epsilon E_x; \quad \frac{\partial H_x}{\partial z} - i\beta H_z = i\omega\epsilon_0\epsilon E_y; \quad i\beta H_y = i\omega\epsilon_0\epsilon Ez \tag{C.6}$$

The system provides two sets of self-consistent solutions with different polarization properties of the propagating waves. The first set are the transverse magnetic (TM) modes, where only the field components E_x, E_z and H_y are nonzero, and the second set the transverse electric (TE) modes, with only H_x , H_z and E_y being nonzero.

For TM mode, the system of equations reduces to

$$E_x = -i\frac{1}{\omega\epsilon_0\epsilon}\frac{\partial H_y}{\partial z}; \quad E_z = -\frac{\beta}{\omega\epsilon_0\epsilon}H_y \tag{C.7}$$

and the wave equation for TM mode is

$$\frac{\partial^2 H_y}{\partial z^2} + (k_o^2\epsilon - \beta^2)H_y = 0 \tag{C.8}$$

For TE mode, an analogous set of equations can be written

$$H_x = i\frac{1}{\omega\mu_0}\frac{\partial E_y}{\partial z}; \quad H_z = \frac{\beta}{\omega\mu_0}E_y \tag{C.9}$$

and the wave equation for TE mode is

$$\frac{\partial^2 E_y}{\partial z^2} + (k_o^2\epsilon - \beta^2)E_y = 0 \tag{C.10}$$

C.1 SPP at Single Interface

SPP waves are sustained at the interface between a metal with dielectric function $\epsilon_m(\omega)$ (Re[$\epsilon_m(< 0)$]) and a dielectric with positive real dielectric constant ϵ_d for TM polarization.

The equations set C.7 can be written for both inside the metal

$$H_y = A_m e^{i\beta x} e^{k_{z,m} z} \tag{C.11}$$

$$E_x = -iA_m \frac{1}{\omega \epsilon_0 \epsilon_m} k_{z,m} e^{i\beta x} e^{k_{z,m} z} \tag{C.12}$$

$$E_z = -A_m \frac{\beta}{\omega \epsilon_0 \epsilon_m} e^{i\beta x} e^{k_{z,m} z} \tag{C.13}$$

and inside the dielectric

$$H_y = A_d e^{i\beta x} e^{-k_{z,d} z} \tag{C.14}$$

$$E_x = iA_d \frac{1}{\omega \epsilon_0 \epsilon_d} k_{z,d} e^{i\beta x} e^{-k_{z,d} z} \tag{C.15}$$

$$E_z = -A_d \frac{\beta}{\omega \epsilon_0 \epsilon_d} e^{i\beta x} e^{-k_{z,d} z} \tag{C.16}$$

where $k_{z,m}$ and $k_{z,d}$ are the wave vectors perpendicular to the direction of propagation in the metal and dielectric, respectively. Continuity of y-component of the magnetic field and z-component of the electric field at the interface results in $A_m = A_d$ and

$$\frac{\epsilon_d}{\epsilon_m} = -\frac{k_{z,d}}{k_{z,m}} \tag{C.17}$$

The wave equation C.8 for H_y further yields

$$k_{z,d}^2 = \beta^2 - k_0^2 \epsilon_d; \quad k_{z,m}^2 = \beta^2 - k_0^2 \epsilon_m \tag{C.18}$$

Combining this with (C.17) yields the dispersion relation for the SPP wave at a single interface

$$\beta = k_0 \sqrt{\frac{\epsilon_m \epsilon_d}{\epsilon_m + \epsilon_d}} \tag{C.19}$$

C.2 SPP in Multilayer Structure

In a multilayer structure like an insulator layer sandwiched between two metal layers (MIM) or metal sandwiched between insulating layers (IMI), each interface of metal and dielectric can sustain a bound SPP wave. As the separation between the two interfaces becomes comparable or smaller than the decay length, the two modes interact with each other giving rise to coupled SPP mode. The TM modes in such a sandwiched structure can be described by the using the above equations. The requirement of continuity of H_y and E_x leads to a linear system of coupled equations that ultimately results in an implicit expression for the dispersion relation

$$e^{-4k_1 a} = \frac{k_1/\epsilon_1 + k_2/\epsilon_2}{k_1/\epsilon_1 - k_2/\epsilon_2} \frac{k_1/\epsilon_1 + k_3/\epsilon_3}{k_1/\epsilon_1 - k_3/\epsilon_3} \tag{C.20}$$

where the subscripts 1, 2 and 3 denote the three layers of the sandwiched structure (1 representing the center layer with thickness $2a$). Considering the outer layers 1 and 3 have same dielectric response, i.e., $\epsilon_2 = \epsilon_3$ and $k_2 = k_3$, we can write the dispersion relation as a pair of equations as follows:

$$tanh k_1 a = -\frac{k_2 \epsilon_1}{k_1 \epsilon_2} \tag{C.21}$$

$$tanh k_1 a = -\frac{k_1 \epsilon_2}{k_2 \epsilon_1} \tag{C.22}$$

Approximate relations for small or large gap width are provided in Chapter 4.

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VITA

Sourav Dutta was born in Kolkata (nicknamed the *"city of joy"*), India in March 1990. In June 2012, he received his Bachelor of Engineering degree in Electrical Engineering from Jadavpur University, Kolkata. In August 2012, he joined Dr. Azad Naeemi's Nanoelectronics Research Lab in the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA to pursue his PhD degree. Working towards his PhD, he subsequently also received a Master of Science in Electrical and Computer Engineering from Georgia Institute of Technology in May 2014. In the summer of 2016, he was a visiting researcher at IMEC, Belgium.

During his PhD research, Sourav has co-authored over sixteen peer-reviewed journal and international conference publications and has two submitted patent applications. He was awarded the 2009 Kishore Vaigyanik Protsahan Yojana (Young Scientist Encouragement Program) Fellowship while pursuing his Bachelors degree in India. He was the co-recipient of the Best Poster Award at the Annual Conference on Magnetism and Magnetic Materials (MMM) in October 2016. His primary area of research has been on modeling and simulation of Spintronic devices and interconnects for Beyond-CMOS application with special focus on spin waves and skyrmions which was funded by and in collaboration with Intel. He is also actively involved in a collaborative research with IMEC and EPFL, Switzerland on developing plasmonic logic for Boolean and non-Boolean computing.